IGBT Gate Drive Guidelines

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It is important to use an appropriate gate voltage and gate resistance to turn an IGBT on and off. If the gate resistance used is too high, then the IGBT switching losses may be excessive. The same is true if the gate voltage is too low. A lower gate voltage can have a more detrimental effect on the IGBT. If the gate voltage is low enough, the IGBT may pull out of saturation and operate in the linear region. When this occurs, the conduction loss in the IGBT is tremendous. The effect is similar to a low voltage short circuit condition. This problem is compounded if a large gate resistance is also used. If the IGBT is not properly driven, this problem may also be seen during turn on if the reverse recovery current from a free wheeling diode forces the IGBT to operate in the linear mode.

If hte gate reistance used is too low, then the IGBT fast switching may lead to excessive EMI. The same is true if the gate voltage is too high. The following example is provided to better understand the effects of gate voltage and gate drive resistance.

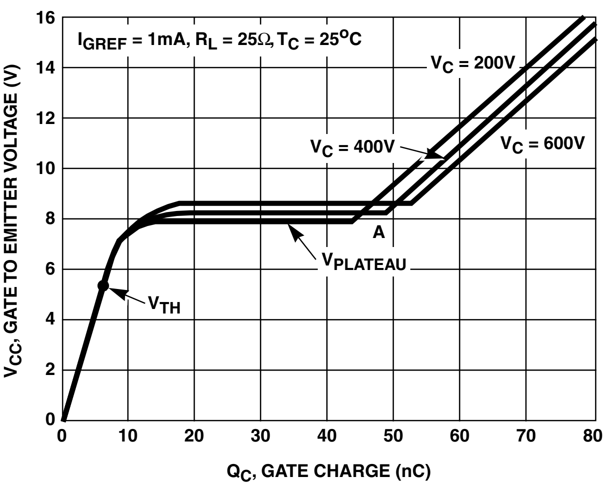

FIGURE 1.

1. Set the collector-emitter di/dt such that the peak reverse recovery current from the diode is less than 3 times the rated current of the IGBT.
2. Using the gate charge curve along with the turn-on time restrictions, the maximum gate resistance is determined in the following way:
   Specify the maximum turn-on time allowable (the longer the turn-on time, the higher the turn-on losses). For this example, use 100ns.
   Specify the gate voltage used. For this example, use 15V. From the gate charge curve, determine the minimum gate charge required. For example, using the gate charge curve with V_{CE} = 400V, point "A" in Figure 1 represents the minimum gate charge required to turn-on the device (for this example, 48nC).
3. To determine the maximum gate resistance, use the plateau voltage associated with the $V_{CE(SAT)}$ condition of your circuit. Subtract this voltage from the applied gated drive voltage (15V - 8V = 7V). This represents the voltage available to provide current to charge and discharge the gate.
   Determine the gate current required 48nC/100ns = 480mA.
   Determine the maximum gate resistor 7V/480mA = 14.6Ω.
4. The minimum gate resistor may be limited by the gate driver or EMI issues.

Turn-off is mainly controlled by the internal device physics. A gate resistor that is too large in value will cause the turn-off energy to increase. Referring to the gate charge curve, we see that under the given conditions, only 8V is available to extract charge from the gate. If we design for a turn-off delay of 150ns while using the same 14.6Ω turn-on gate resistance, then the gate drive circuit must sink 520mA. As long as this time is shorter than the delay time provided in the data sheet, the value of E_{OFF} will not be detrimentally affected. If this time is longer than the delay time provided in the data sheet then the E_{OFF} will be higher than predicted.

Gate resistance validation:

Total gate charge ÷ Design turn-off delay time = required gate current.

Available gate voltage ÷ required gate current = maximum gate resistance.

Required gate current: 78nC/150ns = 0.52A
Maximum gate resistance: 8V/0.52 = 15.4Ω

To illustrate the effect of excess gate resistance on-turn on and turn-off refers to Figures 2 and 3.

For characterization of this IGBT, a gate resistance of 10Ω is used. Notice that with 15V on the gate and at 12A (the current rating for this IGBT) decreasing the gate resistance does not decrease turn-off losses below that with 10Ω. However, turn on losses are reduced.

The turn-on losses, E_{ON2}, represented in the data sheet are the losses including the reverse recovery of a free wheeling diode. This is representative of the losses in a boost PFC. These losses are not only dependent on gate voltage and gate resistance, but also diode temperature as illustrated in Figure 4. If the IGBT is operating in a circuit such as a 2 switch forward and will not turn-on into a freewheeling diode, E_{ON1} is provided. E_{ON1} is NOT dependent on temperature. It is, however, dependent on gate voltage and gate resistance.

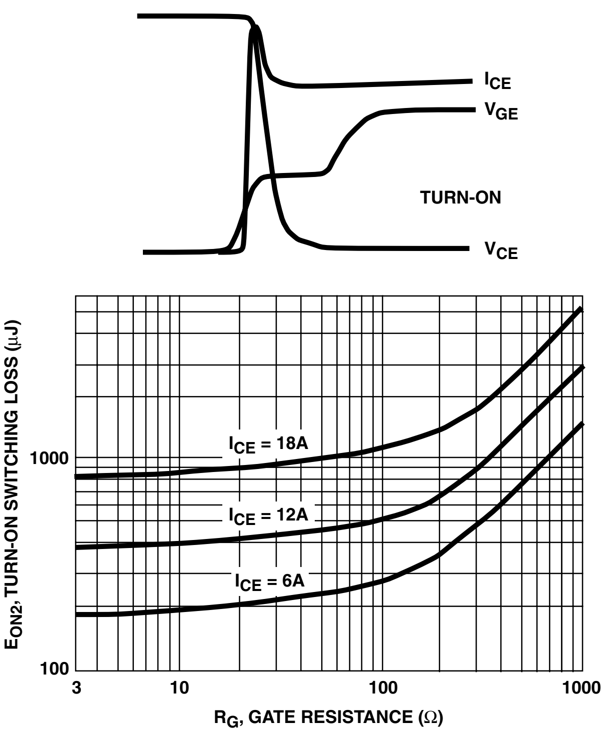

FIGURE 2. TURN-ON

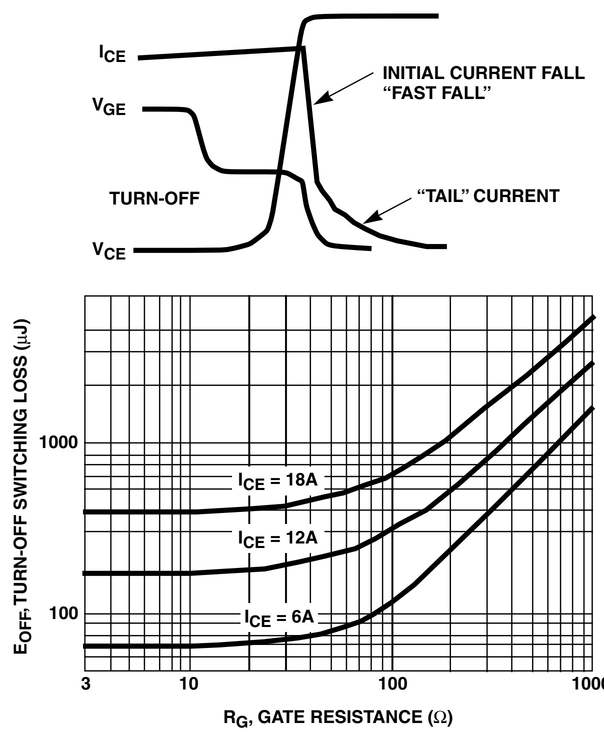

FIGURE 3. TURN-OFF

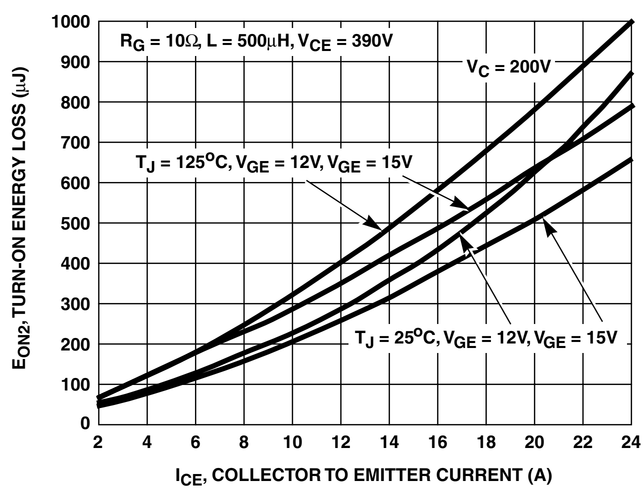

FIGURE 4.

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