

74HC10-Q100; 74HCT10-Q100

Triple 3-input NAND gate

Rev. 1 — 21 February 2013

Product data sheet

1. General description

The 74HC10-Q100; 74HCT10-Q100 is a triple 3-input NAND gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

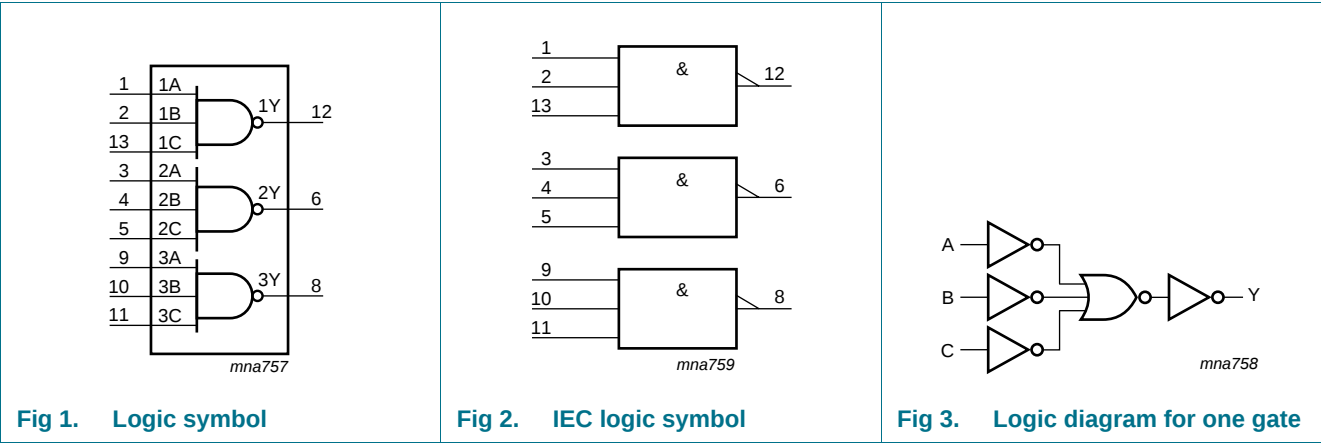
- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD7A
- Input levels:
 - ◆ For 74HC10-Q100: CMOS level
 - ◆ For 74HCT10-Q100: TTL level
- ESD protection:
 - ◆ MIL-STD-883, method 3015 exceeds 2000 V
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V ($C = 200\text{ pF}$, $R = 0\text{ }\Omega$)
- Multiple package options

3. Ordering information

Table 1. Ordering information

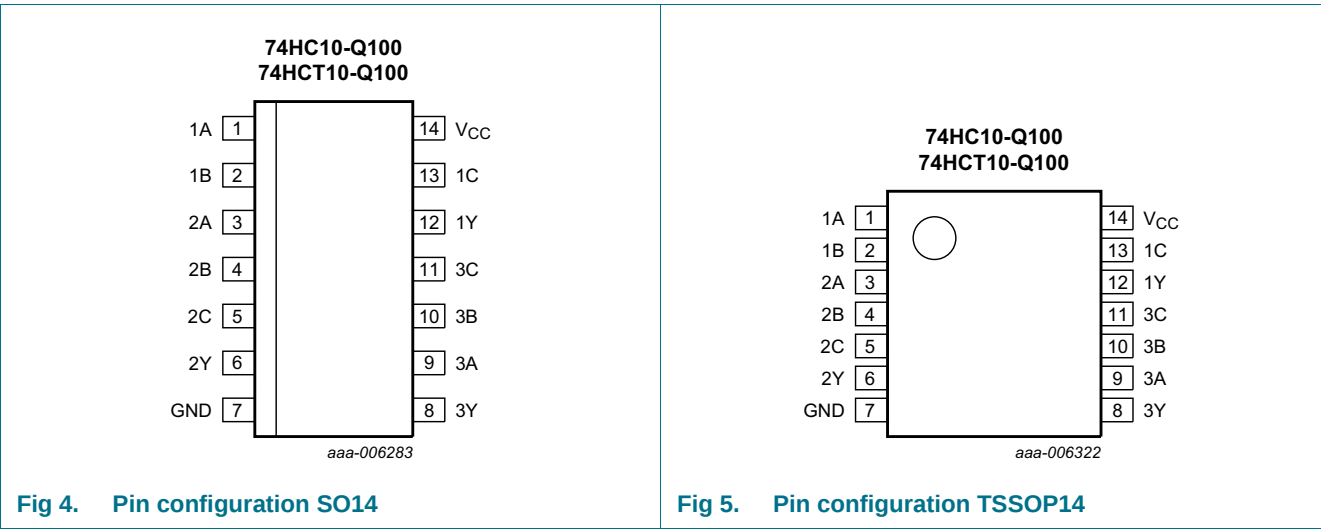
Type number	Package			
	Temperature range	Name	Description	Version
74HC10D-Q100 74HCT10D-Q100	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HC10PW-Q100 74HCT10PW-Q100	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

4. Functional diagram



5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A	1, 3, 9	data input
1B, 2B, 3B	2, 4, 10	data input
GND	7	ground (0 V)
1C, 2C, 3C	13, 5, 11	data input
1Y, 2Y, 3Y	12, 6, 8	data output
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function selection^[1]

Input			Output
nA	nB	nC	nY
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	^[1] -	±20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	^[1] -	±20	mA
I_O	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	-	±25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	SO14 and TSSOP14 packages	^[2] -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
For TSSOP14 package P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC10-Q100			74HCT10-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC10-Q100										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = −20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = −20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = −20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = −4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = −5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	2.0	-	20	-	40	μA

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT10-Q100										
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
		$I_O = -20 \mu\text{A}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4.0 \text{ mA}$	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
		$I_O = 20 \mu\text{A}; V_{CC} = 4.5 \text{ V}$	-	0	0.1	-	0.1	-	0.1	V
I_I	input leakage current	$V_I = V_{CC} \text{ or GND}; V_{CC} = 5.5 \text{ V}$	-	-	± 0.1	-	± 1	-	± 1	μA
I_{CC}	supply current	$V_I = V_{CC} \text{ or GND}; I_O = 0 \text{ A}; V_{CC} = 5.5 \text{ V}$	-	-	2.0	-	20	-	40	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}; I_O = 0 \text{ A};$ other inputs at $V_{CC} \text{ or GND};$ $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	150	540	-	675	-	735	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristicsGND = 0 V; $C_L = 50 \text{ pF}$; for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C			−40 °C to +125 °C		Unit
			Min	Typ	Max	Max (85 °C)	Max (125 °C)	
74HC10-Q100								
t _{pd}	propagation delay	nA, nB to nY; see Figure 6	[1]					
		V _{CC} = 2.0 V	-	30	95	120	145	ns
		V _{CC} = 4.5 V	-	11	19	24	29	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	9	-	-	-	ns
		V _{CC} = 6.0 V	-	9	16	20	25	ns
t _t	transition time	see Figure 6	[2]					
		V _{CC} = 2.0 V	-	19	75	95	110	ns
		V _{CC} = 4.5 V	-	7	15	19	22	ns
		V _{CC} = 6.0 V	-	6	13	16	19	ns
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC}	[3]	-	12	-	-	pF

Table 7. Dynamic characteristics
GND = 0 V; C_L = 50 pF; for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +125 °C		Unit	
			Min	Typ	Max	Max (85 °C)	Max (125 °C)		
74HCT10-Q100									
t _{pd}	propagation delay	nA, nB to nY; see Figure 6	[1]						
		V _{CC} = 4.5 V	-	14	24	30	36	ns	
		V _{CC} = 5.0 V; C _L = 15 pF	-	11	-	-	-	ns	
t _t	transition time	V _{CC} = 4.5 V; see Figure 6	[2]	-	7	15	19	22	ns
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC} – 1.5 V	[3]	-	14	-	-	-	pF

- [1] t_{pd} is the same as t_{PHL} and t_{PLH}.
- [2] t_t is the same as t_{THL} and t_{TLH}.
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
P_D = C_{PD} × V_{CC}² × f_i × N + Σ (C_L × V_{CC}² × f_o) where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
Σ (C_L × V_{CC}² × f_o) = sum of outputs.

11. Waveform and test circuit

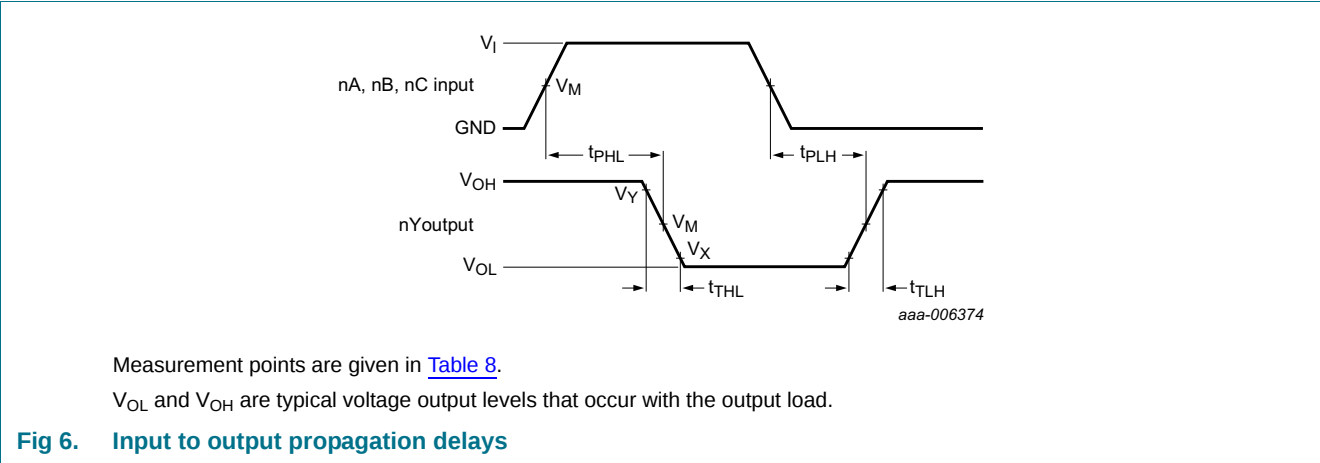
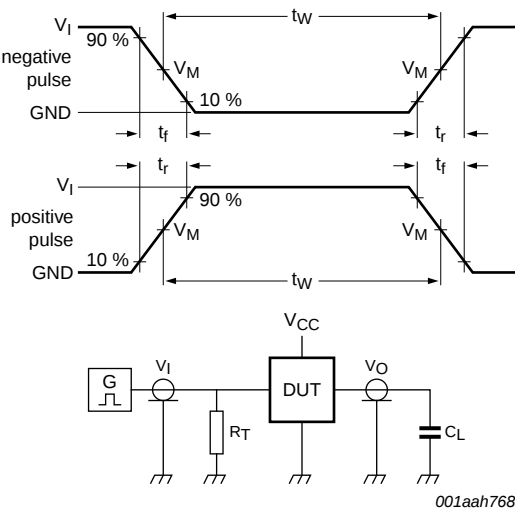


Table 8. Measurement points

Type	Input	Output		
	V _M	V _M	V _X	V _Y
74HC10-Q100	0.5V _{CC}	0.5V _{CC}	0.1V _{CC}	0.9V _{CC}
74HCT10-Q100	1.3 V	1.3 V	0.1V _{CC}	0.9V _{CC}



Test data is given in [Table 9](#).
Definitions test circuit:
 R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.
 C_L = load capacitance including jig and probe capacitance.

Fig 7. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC10-Q100	V_{CC}	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74HCT10-Q100	3.0 V	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

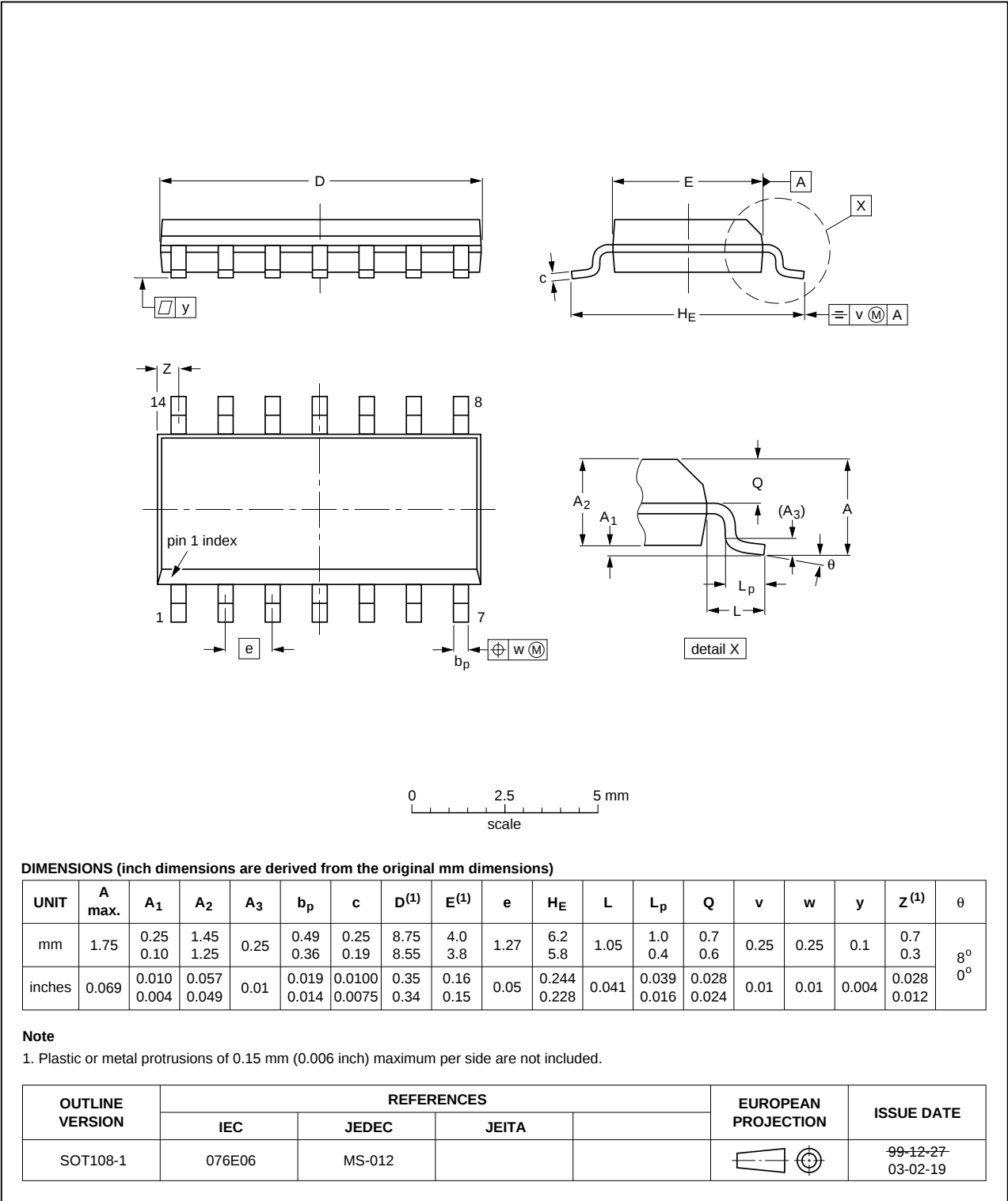


Fig 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

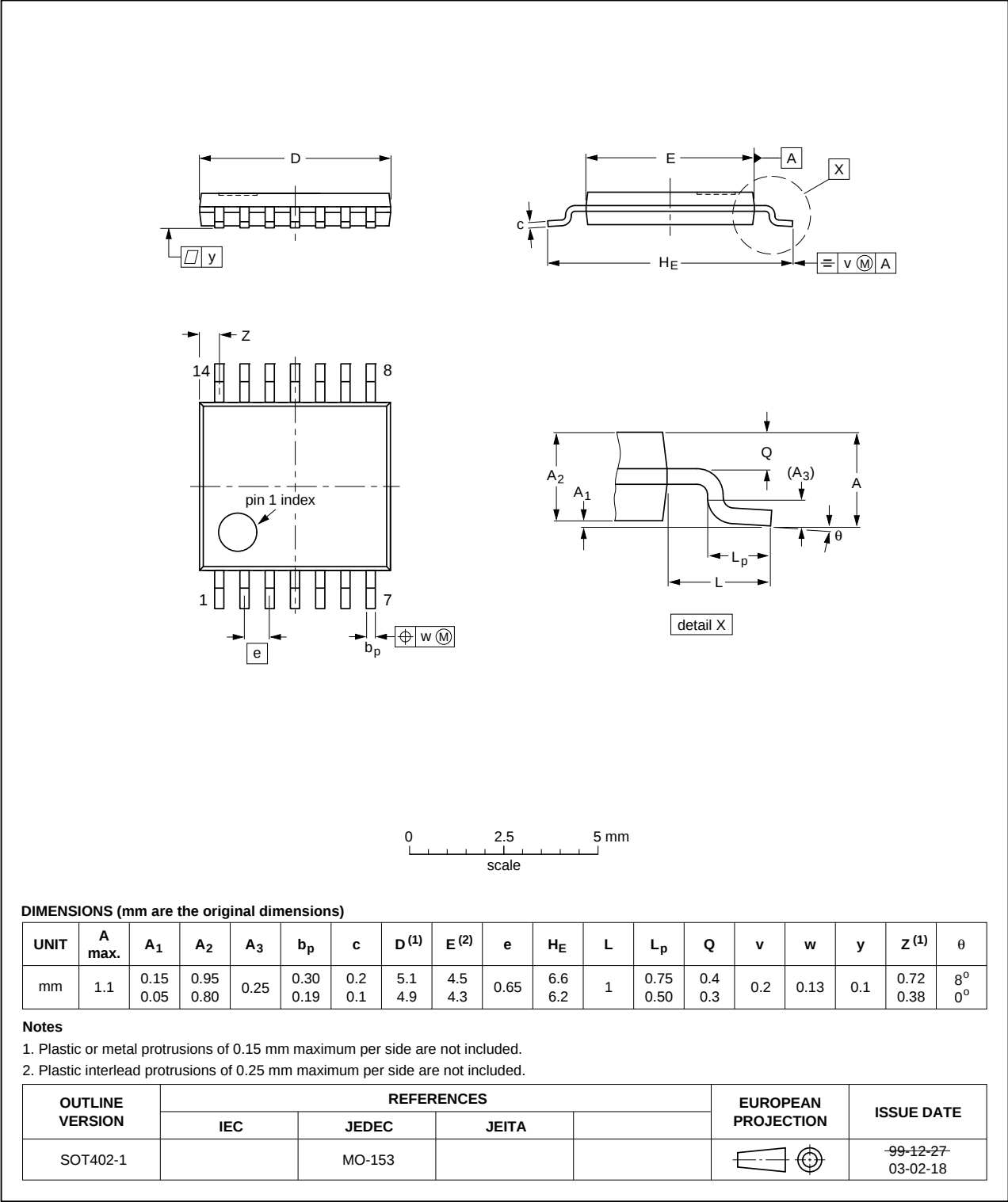


Fig 9. Package outline SOT402-1 (TSSOP14)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
MIL	Military
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT10_Q100 v.1	20130221	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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