

TF796x HF-RFID Reader Layout Design Guide

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ABSTRACT

The following applications note describes some suggested guidelines for use in the laying out the TRF796x family of HF RFID readers. As each customer's implementation will be different, it is the customer's responsibility to ensure that all the proper methodologies and techniques are followed to ensure optimal performance.

1 Design Guide

Figure 1 shows a sample layout as described in this guide.

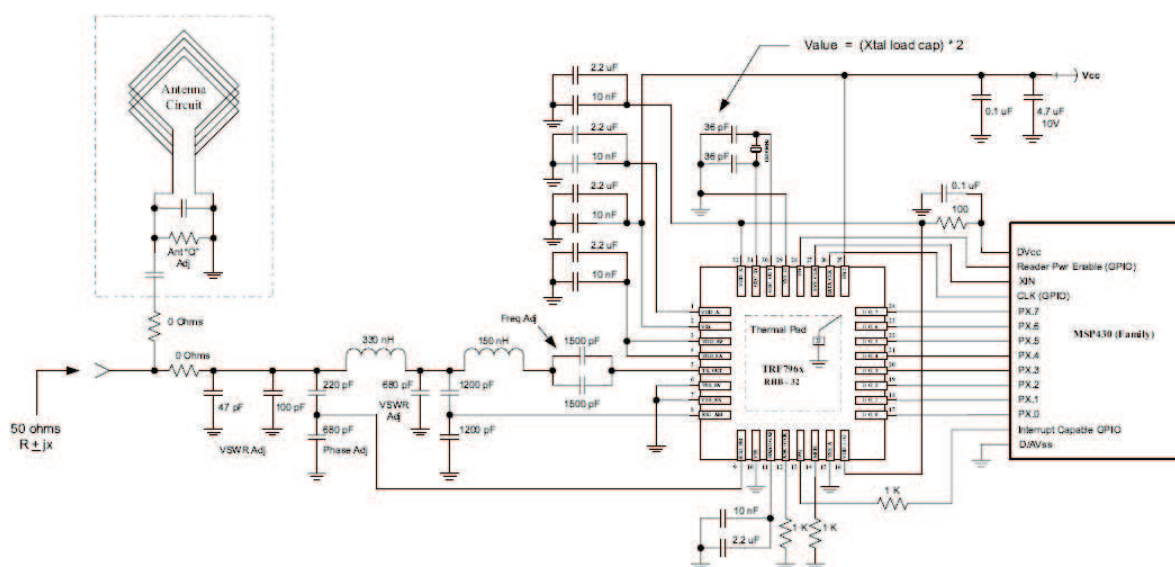
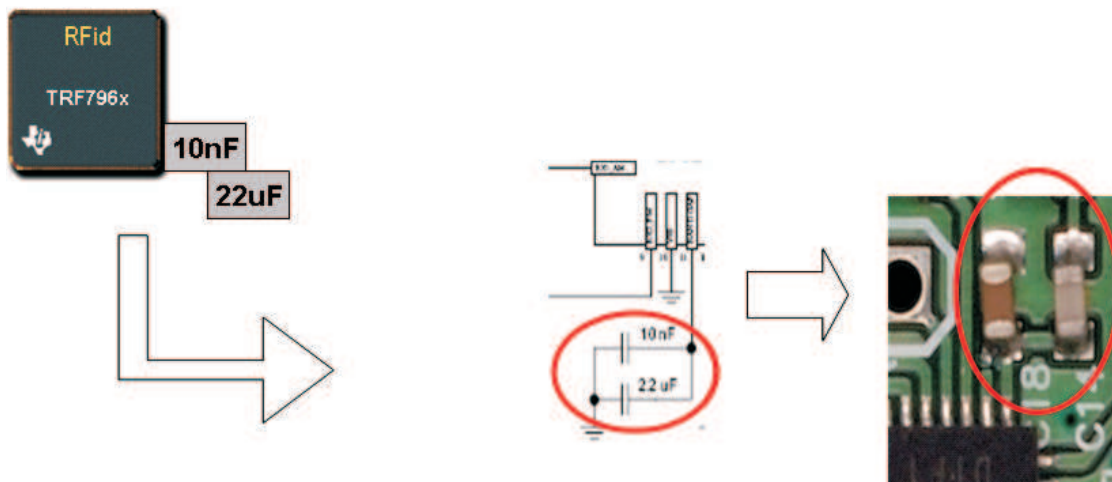
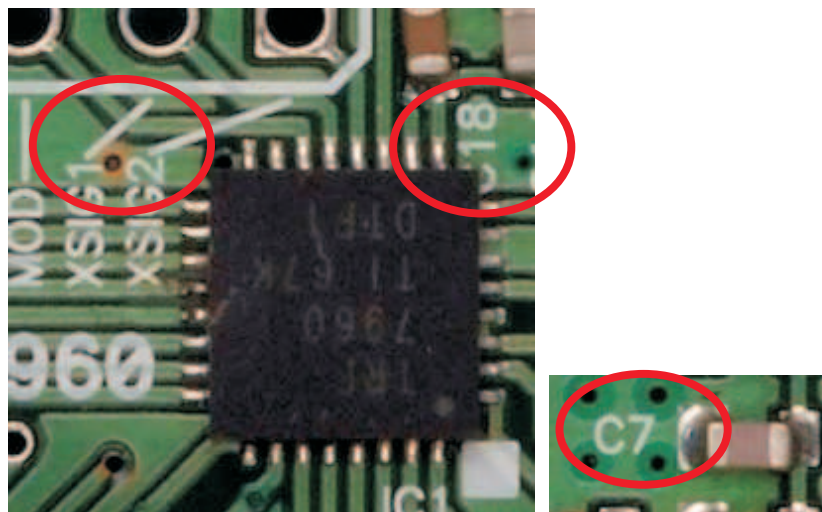


Figure 1. Sample Layout

1. Keep all decoupling caps as close to the IC as possible with the high frequency decoupling cap (10 nF) closer than the low frequency decoupling capacitor (2.2 μ F).



2. Place ground vias as close to the ground side of the capacitors and reader IC pins to minimize any possible ground loops.

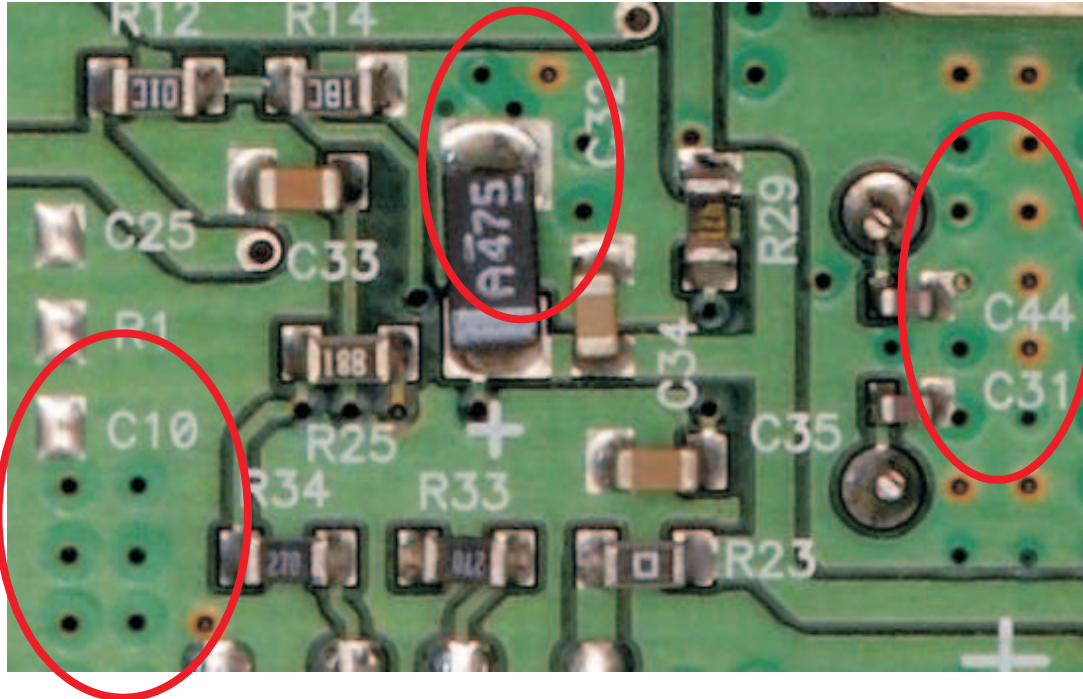


3. Place the two inductors at 90° orientations with respect to each other. (i.e. if the first inductor is laid out in a horizontal manner, the next inductor should be placed in a vertical orientation) this will minimize any coupling between the two.



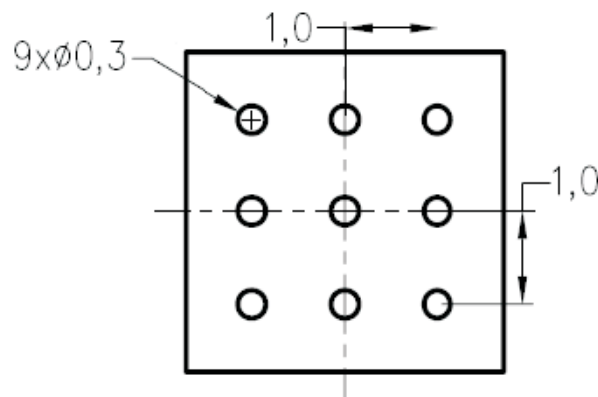
Note: It is not recommend to use any inductor sizes below 0603 as the output power can be compromised. If smaller sized inductors are absolutely necessary, it is up to the customer to confirm output performance.

4. If the crystal is changed from an HC49 to another crystal type the designer should pay close attention to the internal load capacitance and adjust the two external shunt capacitors accordingly. It is recommended that the designer follow the recommendations of the crystal manufacturer for those values.
5. There should be a common ground plane for the digital and analog sections. The multiple ground sections or "islands" should have vias that tie the different sections of the planes together.



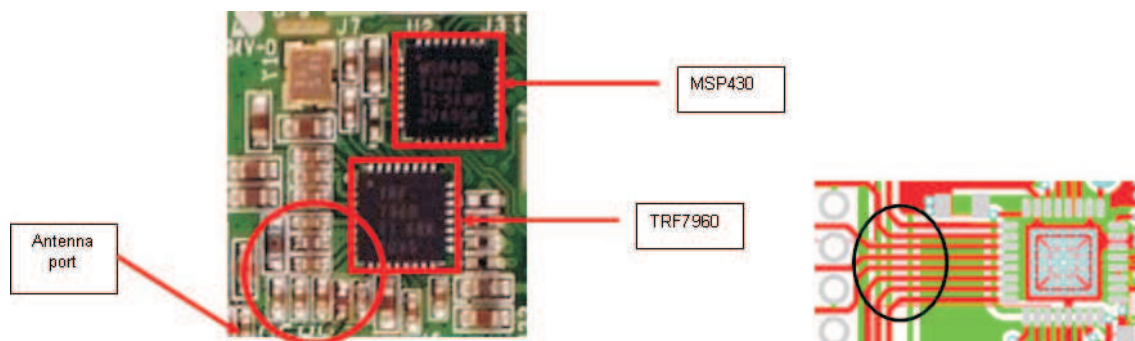
6. Ensure that the PowerPAD™, at the center of the reader IC, is properly laid out (per data sheet, [SLOU186](#)). This will help to dissipate the heat away from the IC. The suggested layout guidelines for the IC (pcb layout, stencil & vias) are shown below:

Example Via Layout Design
may vary depending on constraints



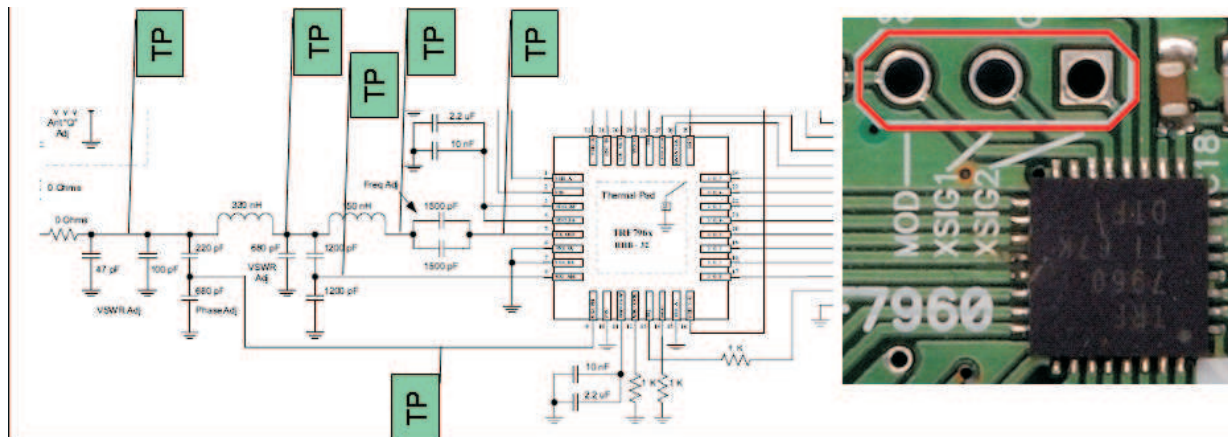
- NOTES:**
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SBAA077, SDA077, and also the Product Data Sheet for specific thermal information, pin requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Lower cutting depths with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their local assembly site for advised design recommendations. Refer to IPC 7520 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via filling recommendations for use vised in the thermal pad.

- Trace line lengths should be minimized whenever possible. Especially, the RF output path, crystal connections and control lines from the reader to the microprocessor. Proper placement of the reader, microprocessor, crystal and RF connection/connector will help facilitate this.



Avoid the following:

- Crossing of digital lines under analog and RF signal lines.
 - Crossing of digital lines with other digital lines whenever possible.
 - If the crossings are unavoidable, 90° crossings should be used to minimize coupling of the lines.
8. Depending on the production test plan, the designer should consider possible implementations of test pads and/or test vias for use during testing. The necessary pads/vias should be placed in accordance with the proposed test plan to help enable easy access to those test points.



9. If the system implementation is complex (i.e. RFID reader module is a subsystem of a greater system with other modules (Bluetooth, WiFi, microprocessors and clocks), special considerations should be taken to ensure that there isn't any noise coupling into the supply lines.
If needed, special filtering/regulator considerations should be used to minimize or eliminate noise in these unique systems. This will ensure optimal RFID reader performance.
10. A suggested reference schematic with the output match from 4 Ω to 50 Ω is provided in the data sheet ([SLOU186](#)) and also the EVM document ([SLOU193](#)). If the customer chooses to follow this suggested schematic, the following conditions should be verified as each implementation will be slightly different.
 - a. Verify the TX output power
 - i. If the desired output is detected, then the component and system matches the EVM.
 - ii. If not detected, then the component value(s) or quality is incorrect.
 - b. Verify the output impedance
 - i. If 50 Ω , then the match is correct and maximum power transfer will be achieved.
 - ii. If not 50 Ω , then it will require some tuning of the output to obtain a 50- Ω output match. Once this is achieved, you will achieve maximum power transfer.
11. Avoid crossing of digital lines under RF signal lines. Also, avoid crossing of digital lines with other digital lines whenever possible. If the crossings are unavoidable, 90° crossings should be used to minimize coupling of the lines.

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