

# FDMC3612

## N-Channel Power Trench® MOSFET

100 V, 12 A, 110 mΩ

### Features

- Max  $r_{DS(on)}$  = 110 mΩ at  $V_{GS} = 10$  V,  $I_D = 3.3$  A
- Max  $r_{DS(on)}$  = 122 mΩ at  $V_{GS} = 6$  V,  $I_D = 3.0$  A
- Low Profile - 1 mm max in Power 33
- 100% UIL Tested
- RoHS Compliant

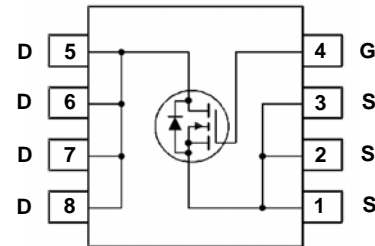
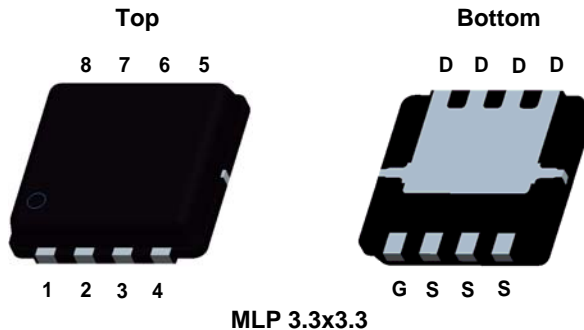


### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

### Applications

- DC - DC Conversion
- PSE Switch



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	100	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous (Package limited) $T_C = 25^\circ\text{C}$	16	A
	-Continuous (Silicon limited) $T_C = 25^\circ\text{C}$	12	
	-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	3.3	
	-Pulsed	15	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	32	mJ
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$	35	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.3	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC3612	FDMC3612	Power 33	13"	12 mm	3000 units

**Electrical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		109		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	2.0	2.5	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-7		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 3.3\text{ A}$		92	110	m $\Omega$
		$V_{GS} = 6\text{ V}, I_D = 3.0\text{ A}$		98	122	
		$V_{GS} = 10\text{ V}, I_D = 3.3\text{ A}, T_J = 125\text{ }^\circ\text{C}$		177	212	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 3.3\text{ A}$		13		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$		662	880	pF
$C_{oss}$	Output Capacitance			40	55	pF
$C_{rss}$	Reverse Transfer Capacitance			23	35	pF
$R_g$	Gate Resistance			1.3		$\Omega$

**Switching Characteristics**

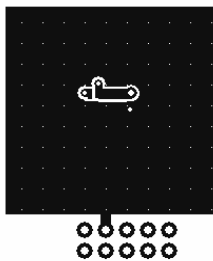
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}, I_D = 3.3\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		7.4	15	ns	
$t_r$	Rise Time			2.8	10	ns	
$t_{d(off)}$	Turn-Off Delay Time			19	34	ns	
$t_f$	Fall Time			2	10	ns	
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\text{ V to }10\text{ V}$		14.4	21	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to }5\text{ V}$	$V_{DD} = 50\text{ V},$ $I_D = 3.3\text{ A}$		7.9	12	nC
$Q_{gs}$	Total Gate Charge				2.3		nC
$Q_{gd}$	Gate to Drain "Miller" Charge				3.7		nC

**Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 3.3\text{ A}$ (Note 2)		0.88	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 2\text{ A}$ (Note 2)		0.77	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 3.3\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		34	55	ns
$Q_{rr}$	Reverse Recovery Charge			37	60	nC

NOTES:

- $R_{\theta JA}$  is determined with the device mounted on a  $1\text{ in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{ in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



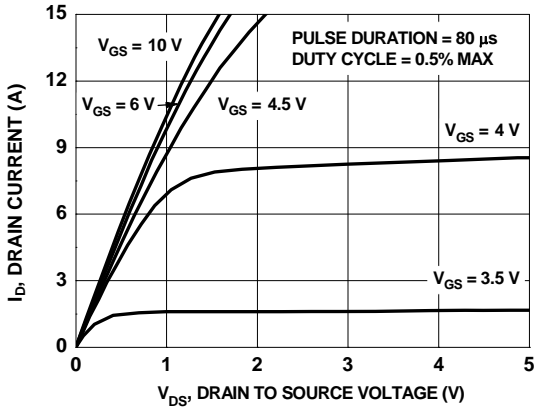
a)  $53\text{ }^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



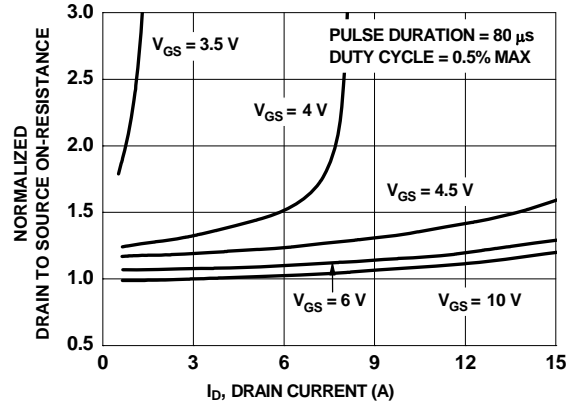
b)  $125\text{ }^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width <  $300\text{ }\mu\text{s}$ , Duty cycle < 2.0%.
- Starting  $T_J = 25\text{ }^\circ\text{C}$ ; N-ch:  $L = 1\text{ mH}, I_{AS} = 8\text{ A}, V_{DD} = 90\text{ V}, V_{GS} = 10\text{ V}$ .

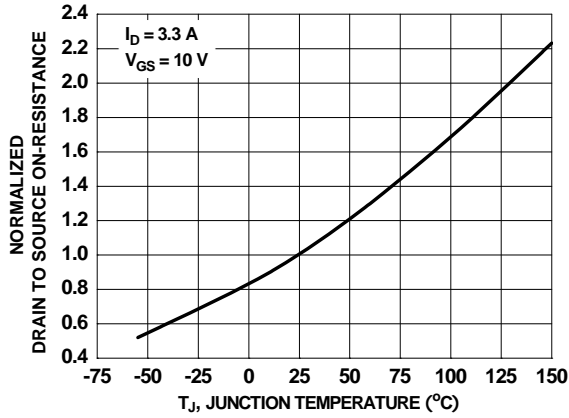
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



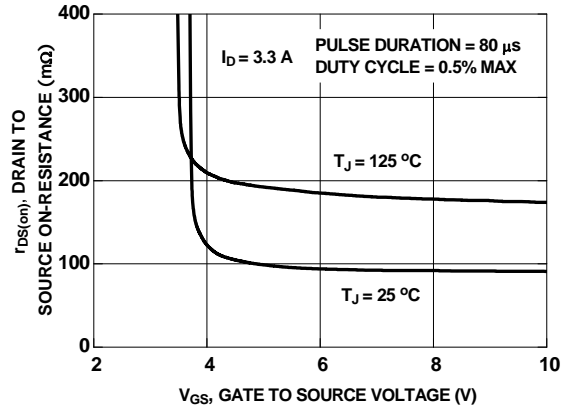
**Figure 1. On Region Characteristics**



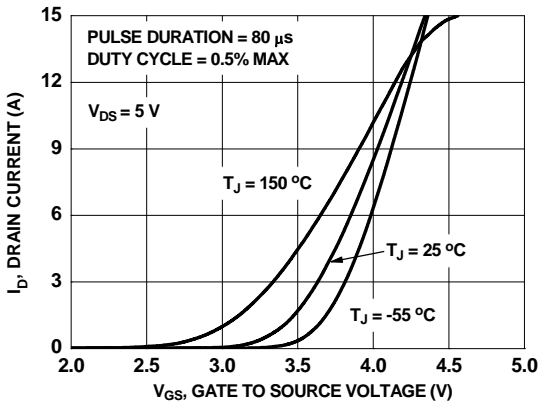
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



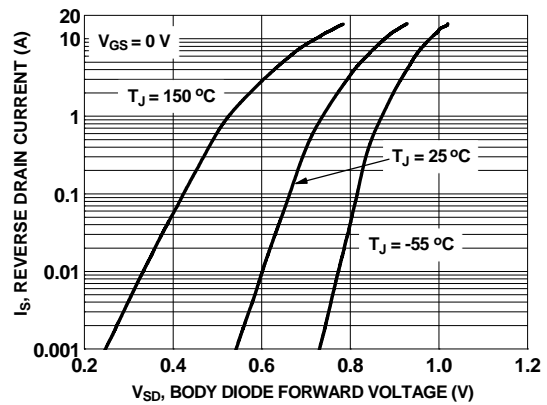
**Figure 3. Normalized On Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

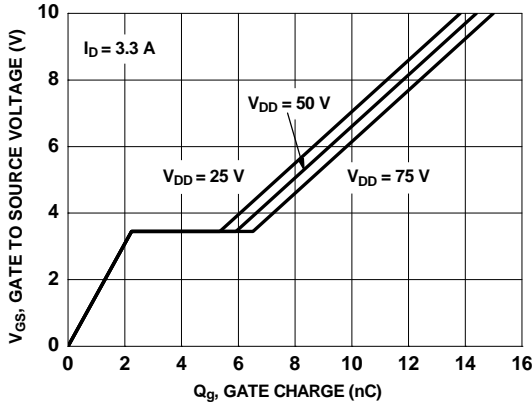


**Figure 5. Transfer Characteristics**

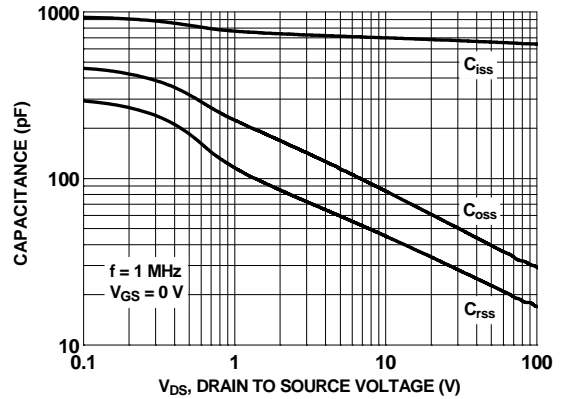


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

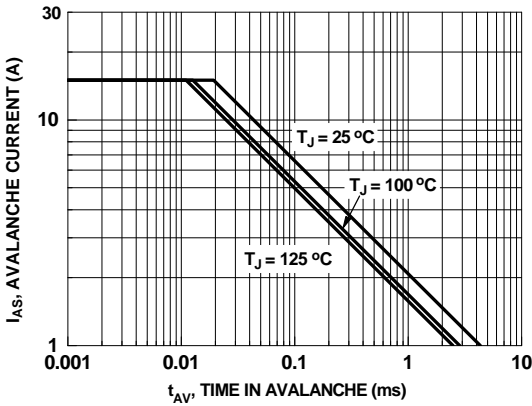
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



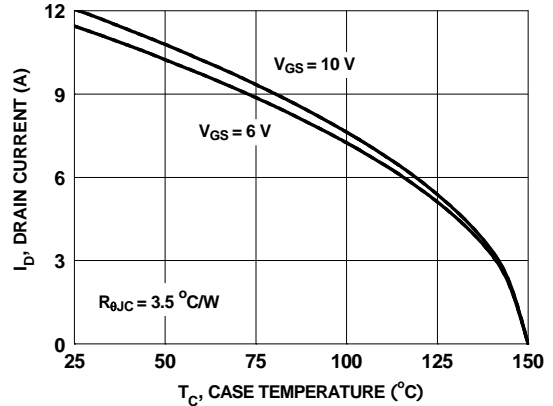
**Figure 7. Gate Charge Characteristics**



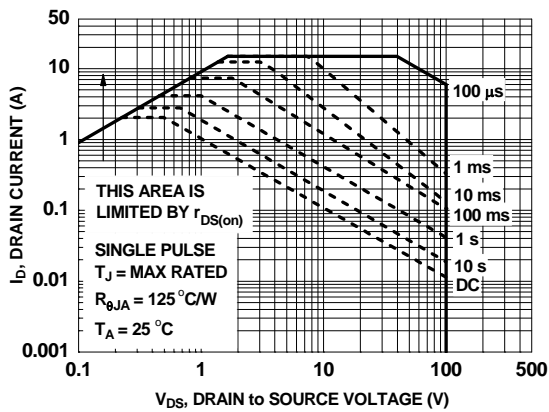
**Figure 8. Capacitance vs Drain to Source Voltage**



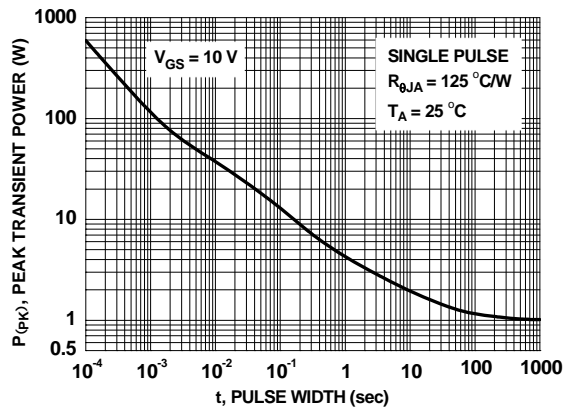
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

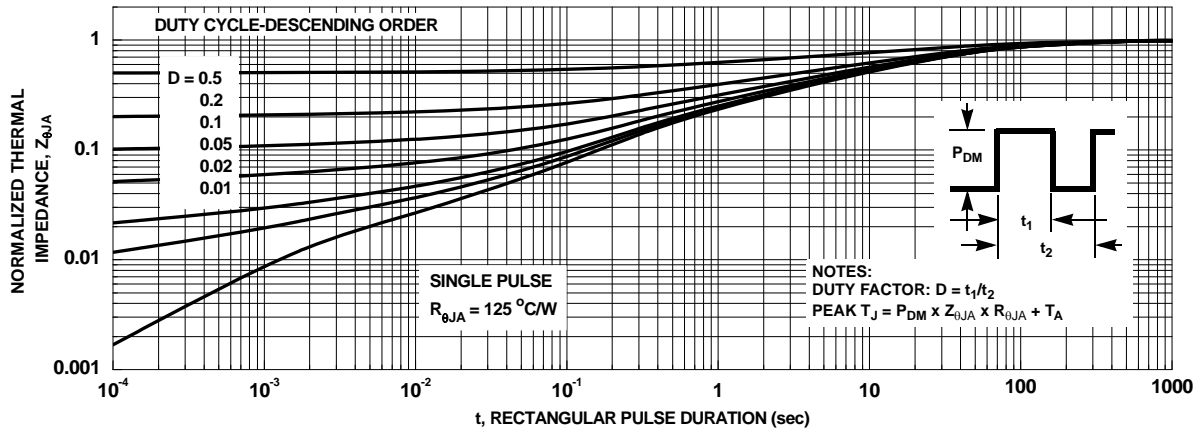


**Figure 11. Forward Bias Safe Operating Area**



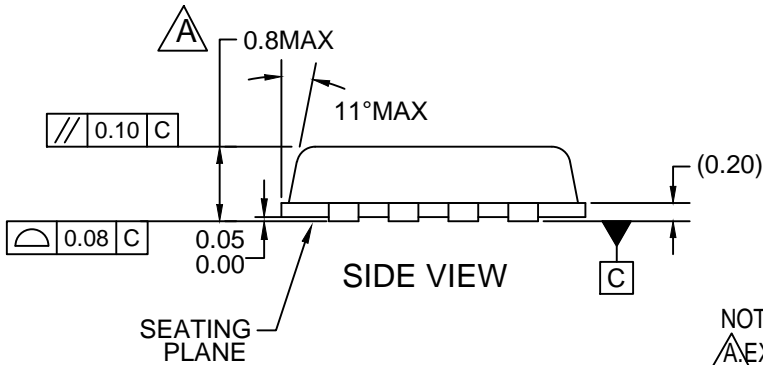
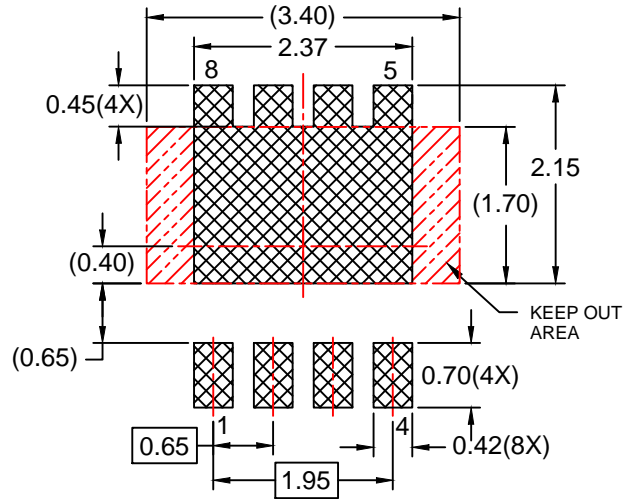
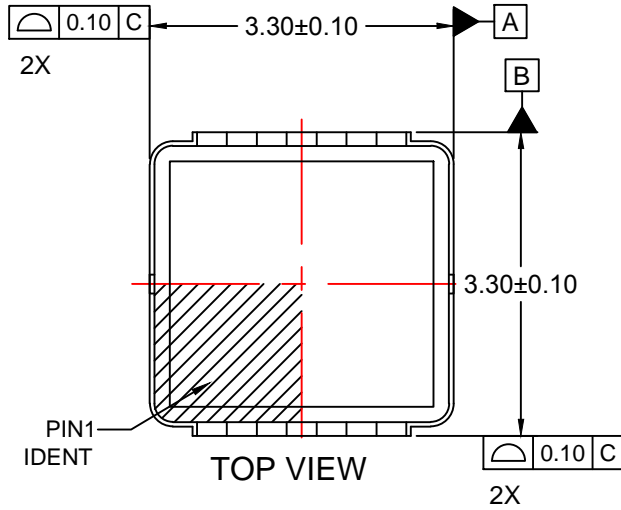
**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**

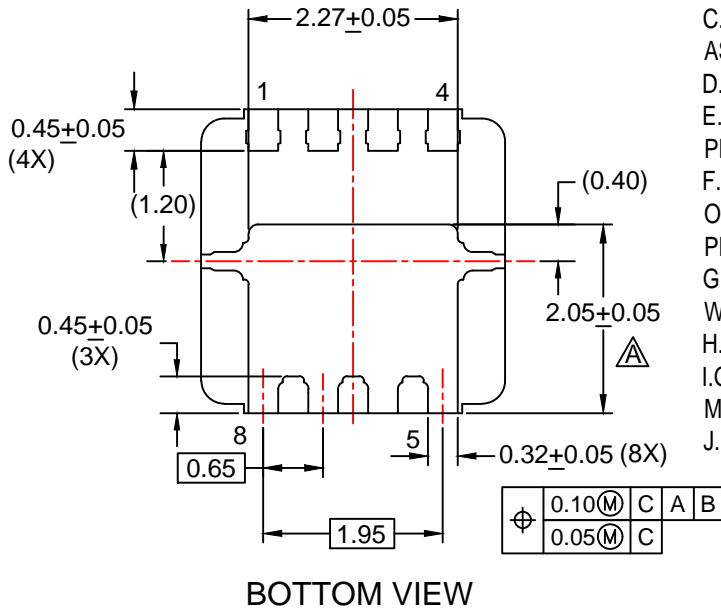
### Dimensional Outline and Pad Layout



### RECOMMENDED LAND PATTERN

#### NOTES:



- A. EXCEPT AS NOTED, PACKAGE CONFORMS TO JEDEC REGISTRATION MO-240 VARIATION BA..
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
- D. SEATING PLANE IS DEFINED BY TERMINAL TIPS ONLY
- E. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATEBURRS.
- F. FLANGE DIMENSIONS INCLUDE INTERTERMINAL FLASH OR PROTRUSION. INTERTERMINAL FLASH OR PROTRUSION SHALL NOT EXCEED 0.25MM PER SIDE.
- G. IT IS RECOMMENDED TO HAVE NO TRACES OR VIA WITHIN THE KEEP OUT AREA.
- H. DRAWING FILENAME: MKT-MLP08Trev3.
- I. GENERAL RADII FOR ALL CORNERS SHALL BE 0.20MM MAX.
- J. FAIRCHILD SEMICONDUCTOR.





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**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

Datasheet Identification	Product Status	Definition
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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