



September 2014

FDMA86151L

Single N-Channel PowerTrench[®] MOSFET

100 V, 3.3 A, 88 mΩ

Features

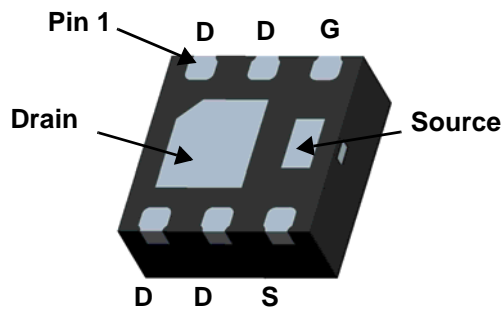
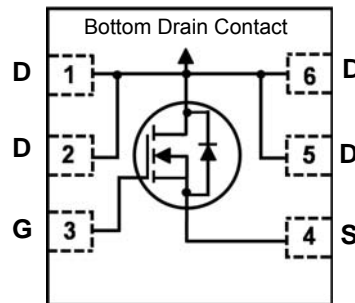
- Max $r_{DS(on)}$ = 88 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 3.3\text{ A}$
- Max $r_{DS(on)}$ = 132 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 2.7\text{ A}$
- Low Profile - 0.8 mm maximum in the new package MicroFET 2x2 mm
- Free from halogenated compounds and antimony oxides
- RoHS Compliant

General Description

This device has been designed to provide maximum efficiency and thermal performance for synchronous buck converters. The low $r_{DS(on)}$ and gate charge provide excellent switching performance.

Application

- DC – DC Buck Converters

**MicroFET 2X2 (Bottom View)**

MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Curre -Continuous $T_A = 25\text{ °C}$ (Note 1a)	3.3	A
	-Pulsed (Note 3)	20	
P_D	Power Dissipation $T_A = 25\text{ °C}$ (Note 1a)	2.4	W
	Power Dissipation $T_A = 25\text{ °C}$ (Note 1b)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	145	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
151	FDMA86151L	MicroFET 2X2	7 "	8 mm	3000 units

Electrical Characteristics $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^{\circ}\text{C}$		69		mV/ $^{\circ}\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$			100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\text{ }\mu\text{A}$	1.0	2.0	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^{\circ}\text{C}$		-6		mV/ $^{\circ}\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 3.3\text{ A}$		60	88	m Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 2.7\text{ A}$		83	132	
		$V_{GS} = 10\text{ V}$, $I_D = 3.3\text{ A}$, $T_J = 125\text{ }^{\circ}\text{C}$		102	150	
g_{FS}	Forward Transconductance	$V_{DD} = 5\text{ V}$, $I_D = 3.3\text{ A}$		8.6		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 50\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		322	450	pF
C_{oss}	Output Capacitance			55	80	pF
C_{rss}	Reverse Transfer Capacitance			3	5	pF
R_g	Gate Resistance		0.1	1.9	3.8	Ω

Switching Characteristics

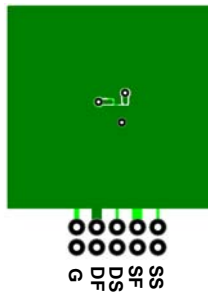
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}$, $I_D = 3.3\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		5.6	12	ns
t_r	Rise Time			1.4	10	ns
$t_{d(off)}$	Turn-Off Delay Time			11	20	ns
t_f	Fall Time			1.6	10	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to } 10\text{ V}$	$V_{DD} = 50\text{ V}$, $I_D = 3.3\text{ A}$	5.2	7.3	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\text{ V to } 4.5\text{ V}$		2.6	3.7	nC
Q_{gs}	Gate to Source Charge			1.1		nC
Q_{gd}	Gate to Drain "Miller" Charge			1.0		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 3.3\text{ A}$ (Note 2)		0.8	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 3.3\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		33	53	ns
Q_{rr}	Reverse Recovery Charge			25	40	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a. 52 $^{\circ}\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper.



b. 145 $^{\circ}\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

3. Pulsed I_d limited by junction temperature, $t_d \leq 10\text{ }\mu\text{s}$, please refer to SOA curve for more details.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

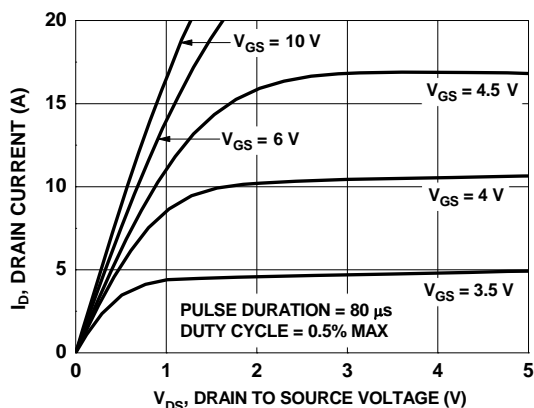


Figure 1. On-Region Characteristics

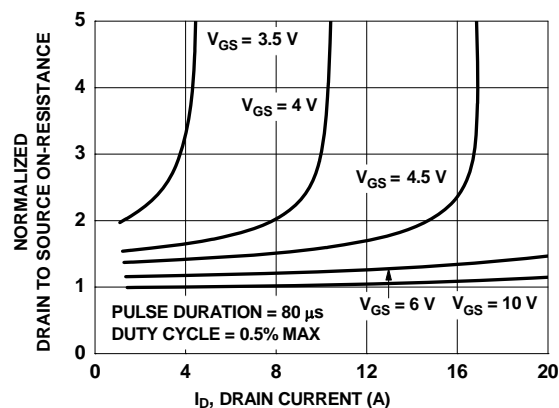


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

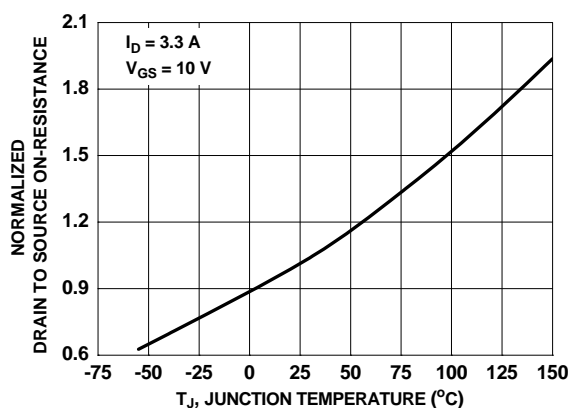


Figure 3. Normalized On-Resistance vs Junction Temperature

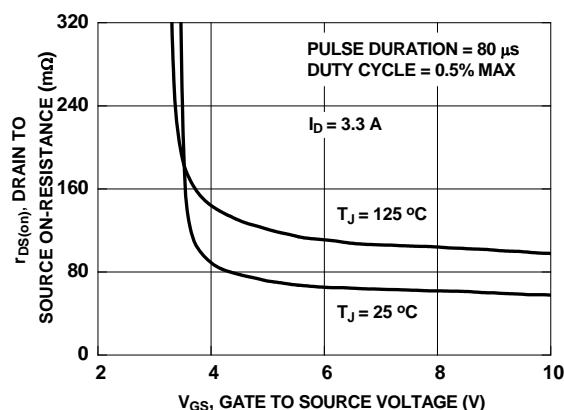


Figure 4. On-Resistance vs Gate to Source Voltage

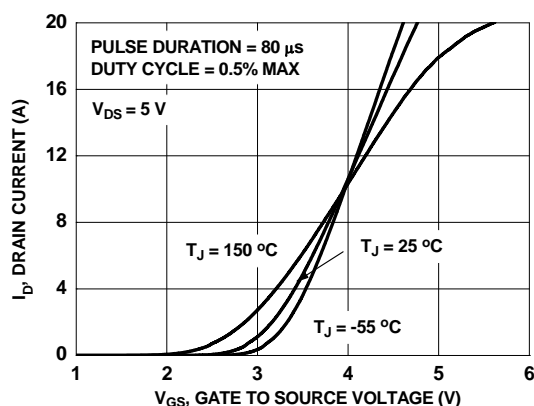


Figure 5. Transfer Characteristics

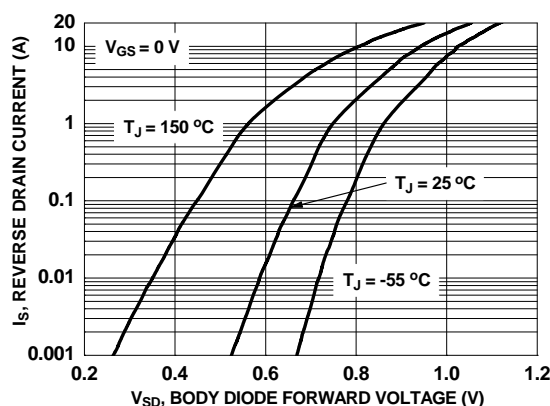


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

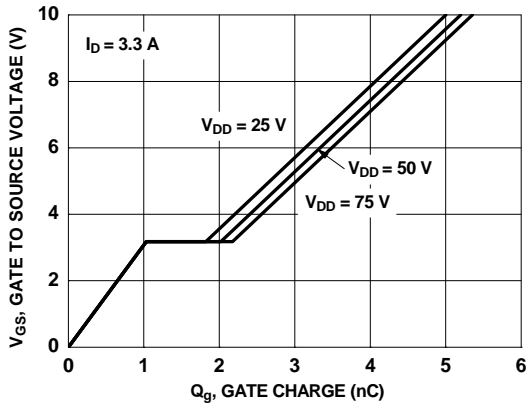


Figure 7. Gate Charge Characteristics

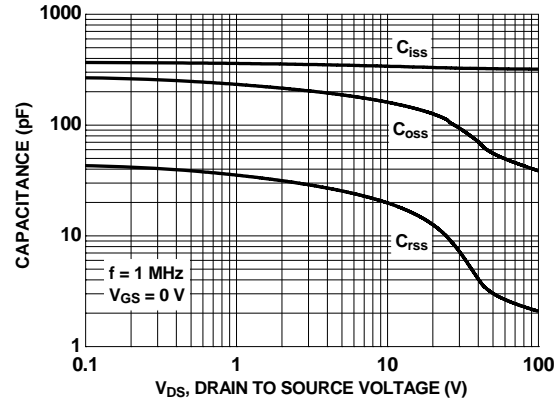


Figure 8. Capacitance vs Drain to Source Voltage

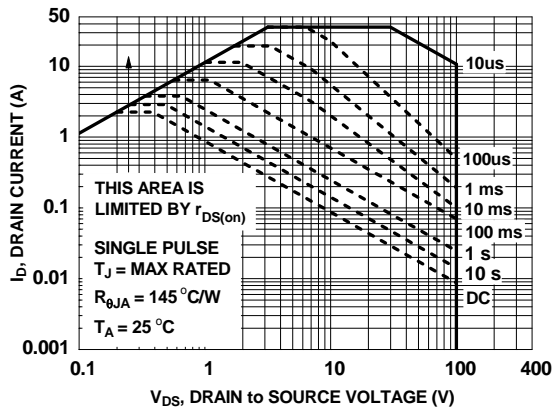


Figure 9. Forward Bias Safe Operating Area

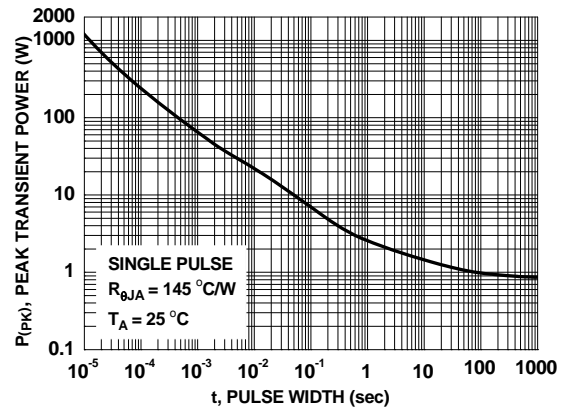


Figure 10. Single Pulse Maximum Power Dissipation

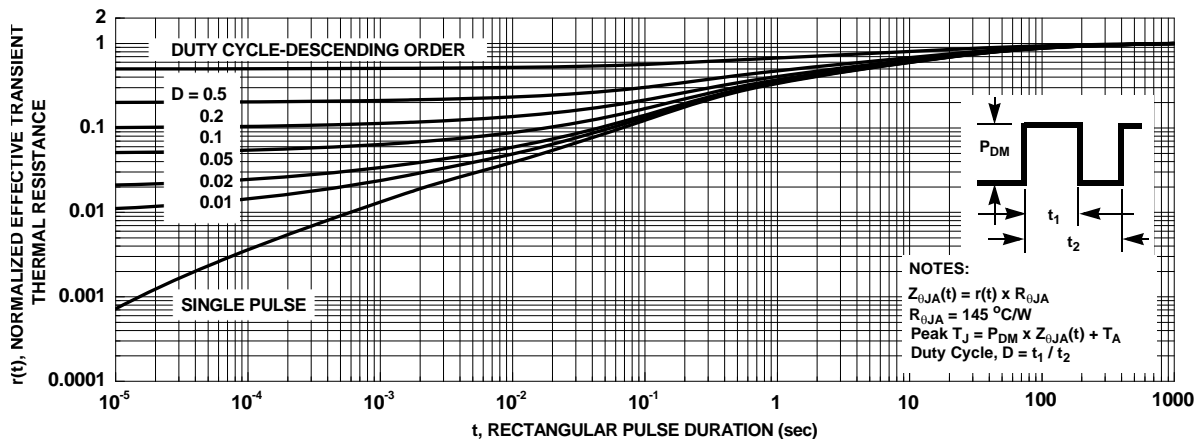
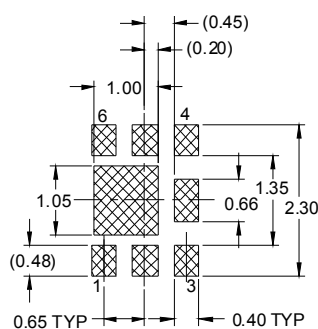
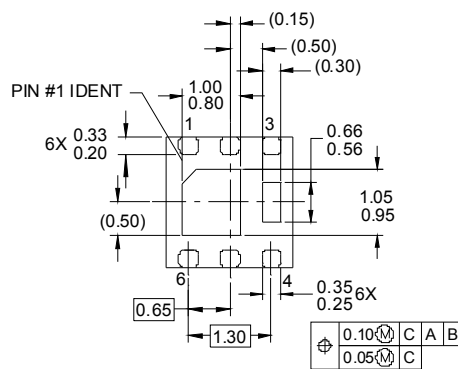
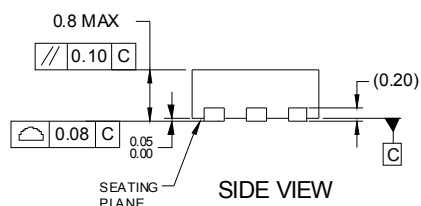
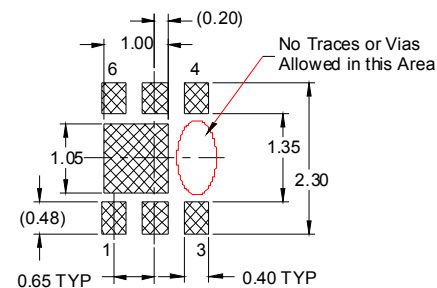
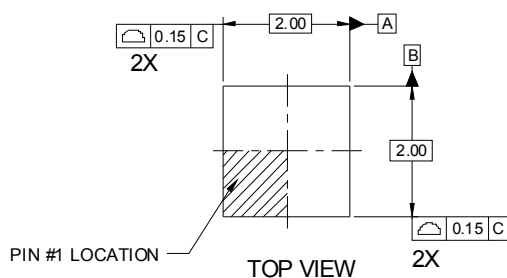


Figure 11. Single Pulse Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout



NOTES:

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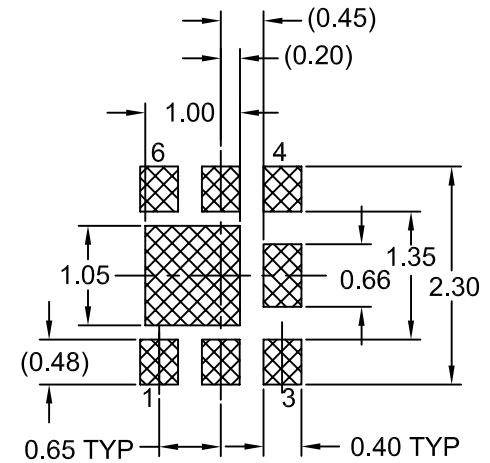
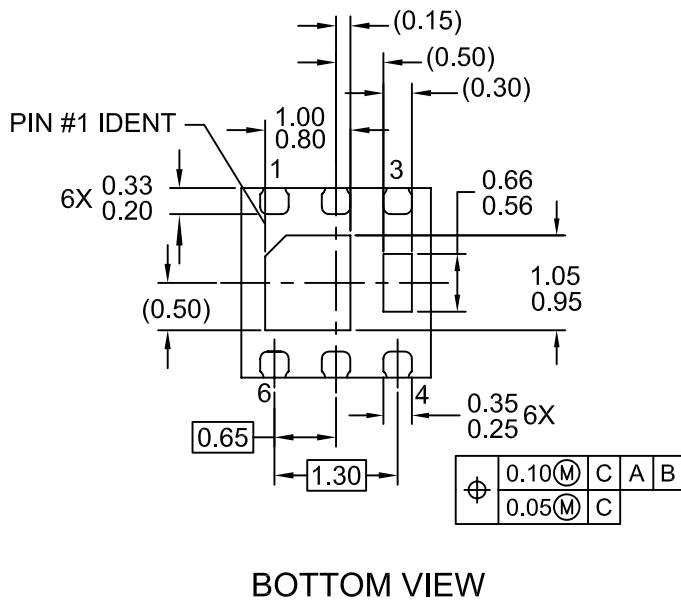
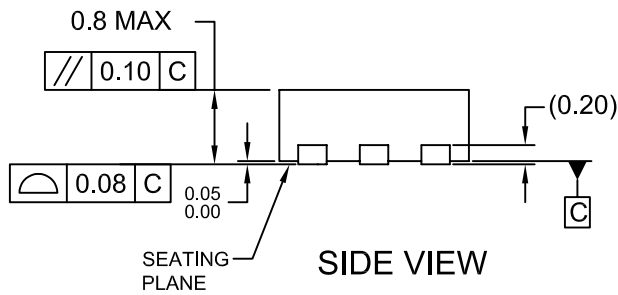
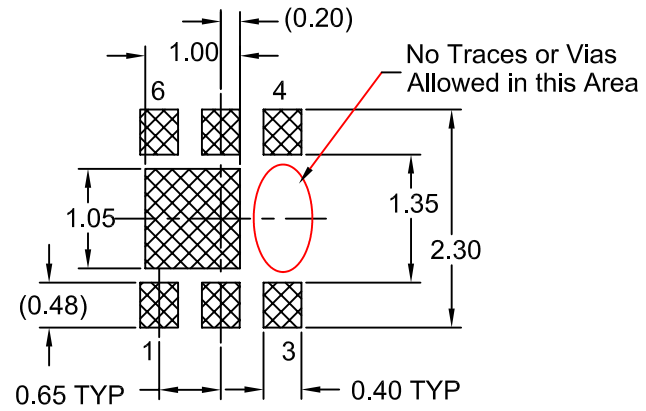
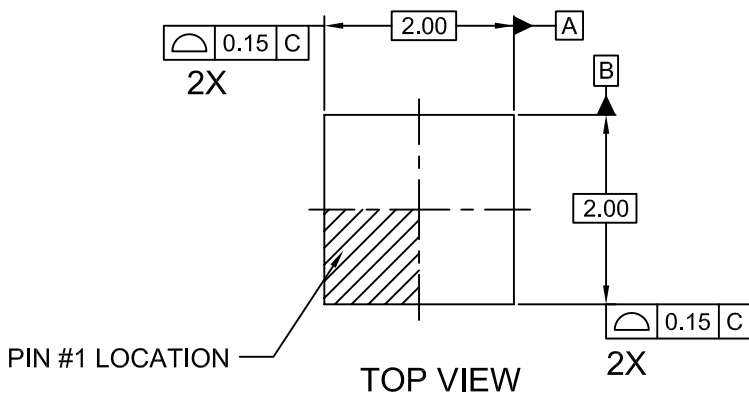
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