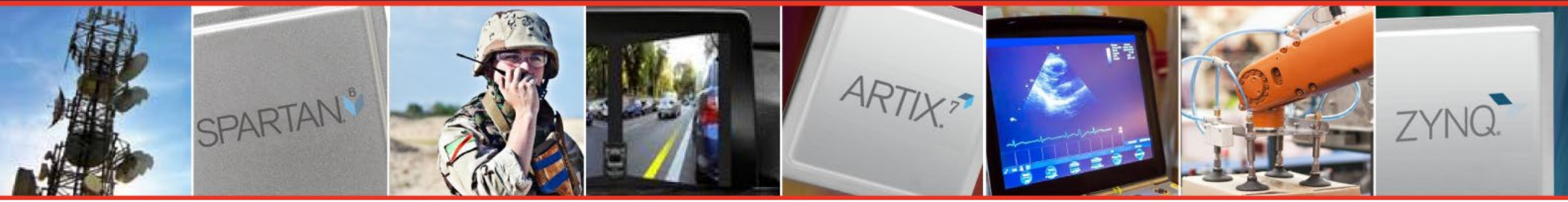
All Programmable Low-End Portfolio
Product Tables and Product Selection Guide



SPARTAN 6 ARTIX 7 ZYNQ

XILINX
ALL PROGRAMMABLE™

Spartan-6 FPGAs

		Spartan®-6 LX FPGAs Optimized for Lowest-Cost Logic, DSP, and Memory (1.2V, 1.0V)								Spartan-6 LXT FPGAs Optimized for Lowest-Cost Logic, DSP, and Memory with High-Speed Serial Connectivity (1.2V)				
	Part Number	XC6SLX4	XC6SLX9	XC6SLX16	XC6SLX25	XC6SLX45	XC6SLX75	XC6SLX100	XC6SLX150	XC6SLX25T	XC6SLX45T	XC6SLX75T	XC6SLX100T	XC6SLX150T
Logic Resources	Slices[1]	600	1,430	2,278	3,758	6,822	11,662	15,822	23,038	3,758	6,822	11,662	15,822	23,038
	Logic Cells[2]	3,840	9,152	14,579	24,051	43,661	74,637	101,261	147,443	24,051	43,661	74,637	101,261	147,443
	CLB Flip-Flops	4,800	11,440	18,224	30,064	54,576	93,296	126,576	184,304	30,064	54,576	93,296	126,576	184,304
Memory Resources	Maximum Distributed RAM (Kb)	75	90	136	229	401	692	976	1,355	229	401	692	976	1,355
	Block RAM (18 Kb each)	12	32	32	52	116	172	268	268	52	116	172	268	268
	Total Block RAM (Kb)[3]	216	576	576	936	2,088	3,096	4,824	4,824	936	2,088	3,096	4,824	4,824
Clock Resources	Clock Management Tiles (CMT)[4]	2	2	2	2	4	6	6	6	2	4	6	6	6
I/O Resources	Maximum Single-Ended Pins	132	200	232	266	358	408	480	576	250	296	348	498	540
	Maximum Differential Pairs	66	100	116	133	179	204	240	288	125	148	174	249	270
Embedded Hard IP Resources	DSP48A1 Slices[5]	8	16	32	38	58	132	180	180	38	58	132	180	180
	Endpoint Block for PCI Express®	—	—	—	—	—	—	—	—	1	1	1	1	1
	Memory Controller Blocks	0	2	2	2	2	4	4	4	2	2	4	4	4
	GTP Low-Power Transceivers	—	—	—	—	—	—	—	—	2	4	8	8	8
Speed Grades	Commercial[10]	-1L, -2, -3	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N
	Industrial[10]	-1L, -2, -3	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-1L, -2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N	-2, -3, -3N
Configuration	Configuration Memory (Mb)	2.7	2.7	3.7	6.4	11.9	19.6	26.5	33.8	6.4	11.9	19.6	26.5	33.8

Package	Body Area	Maximum User I/O: SelectIO™ Interface Pins (GTP Transceivers)[6]												
Chip Scale Packages (CPG): Pb-free, wire-bond, chip scale BGA (0.5 mm ball spacing)														
CPG196[7]	8 x 8 mm	106	106	106										
TQFP Packages (TQG): Pb-free, thin QFP (0.5 mm lead spacing)														
TQG144[7]	20 x 20 mm	102	102											
Chip Scale Packages (CSG): Pb-free, wire-bond, chip scale BGA (0.8 mm ball spacing)														
CSG225[8]	13 x 13 mm	132	160	160										
CSG324	15 x 15 mm		200	232	226	218				190 (2)	190 (4)			
CSG484[9]	19 x 19 mm					320	328	338	338		296 (4)	292 (4)	296 (4)	296 (4)
BGA Packages (FTG): Pb and Pb-free, wire-bond, fine-pitch thin BGA (1.0 mm ball spacing)														
FT(G)256	17 x 17 mm		186	186	186									
BGA Packages (FGG): Pb and Pb-free, wire-bond, fine-pitch BGA (1.0 mm ball spacing)														
FG(G)484[9]	23 x 23 mm				266	316	280	326	338	250 (2)	296 (4)	268 (4)	296 (4)	296 (4)
FG(G)676	27 x 27 mm					358	408	480	498			348 (8)	376 (8)	396 (8)
FG(G)900	31 x 31 mm								576				498 (8)	540 (8)

XMP071 (v1.2)

Notes:
1. Each slice contains four LUTs and eight flip-flops.
2. Spartan-6 FPGA logic cell ratings reflect the increased logic capacity offered by the new 6-input LUT architecture.
3. Block RAM are fundamentally 18Kb in size. Each block can also be used as two independent 9 Kb blocks.
4. Each CMT contains two DCMs and one PLL.
5. Each DSP48A1 slice contains an 18x18 multiplier, an adder, and an accumulator.
6. The LX device pinouts are not compatible with the LXT device pinouts.
7. CPG196 and TQG144 do not have memory controller support. -3N is not available for these packages.
8. CSG225 has X8 memory controller support in the LX9 and LX16 devices. There is no memory controller in the LX4 devices.
9. Devices in the FG(G)484 and CSG484 packages have support for two memory controllers.
10. Devices with -3N speed grade do not support MCB functionality.

Artix-7 FPGAs

		Artix®-7 FPGAs Optimized for Lowest Cost and Lowest Power Applications (1.0V, 0.95V, 0.9V)					
	Part Number	XC7A15T	XC7A35T	XC7A50T	XC7A75T	XC7A100T	XC7A200T
Logic Resources	Logic Cells	16,640	33,280	52,160	75,520	101,440	215,360
	Slices	2,600	5,200	8,150	11,800	15,850	33,650
	CLB Flip-Flops	20,800	41,600	65,200	94,400	126,800	269,200
Memory Resources	Maximum Distributed RAM (Kb)	200	400	600	892	1,188	2,888
	Block RAM/FIFO w/ ECC (36 Kb each)	25	50	75	105	135	365
	Total Block RAM (Kb)	900	1,800	2,700	3,780	4,860	13,140
Clock Resources	CMTs (1 MMCM + 1 PLL)	5	5	5	6	6	10
I/O Resources	Maximum Single-Ended I/O	250	250	250	300	300	500
	Maximum Differential I/O Pairs	120	120	120	144	144	240
Embedded Hard IP Resources	DSP Slices	45	90	120	180	240	740
	PCIe® Gen2[1]	1	1	1	1	1	1
	Analog Mixed Signal (AMS) / XADC	1	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1	1
	GTP Transceivers (6.6 Gb/s Max Rate)[2]	4	4	4	8	8	16
Speed Grades	Commercial	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Extended	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3
	Industrial	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L
	Package[3], [4]	Dimensions (mm)	**Available User I/O**: 3.3V SelectIO™ HR I/O (GTP Transceivers)				
	CPG236	10 x 10	106 (2)	106 (2)	106 (2)		
	CSG324	15 x 15	210 (0)	210 (0)	210 (0)	210 (0)	210 (0)
	CSG325	15 x 15	150 (4)	150 (4)	150 (4)		
	FTG256	17 x 17	170 (0)	170 (0)	170 (0)	170 (0)	170 (0)
	SBG484 / SBV484	19 x 19					285 (4)
Footprint Compatible	FGG484	23 x 23	250 (4)	250 (4)	250 (4)	285 (4)	285 (4)
	FBG484 / FBV484	23 x 23					285 (4)
Footprint Compatible	FGG676	27 x 27				300 (8)	300 (8)
	FBG676 / FBV676	27 x 27					400 (8)
	FFG1156 / FFV1156	35 x 35					500 (16)

XMP086 (v4.7)

CPG: 0.5 mm Wire-bond chip-scale; **CSG**: 0.8 mm Wire-bond chip-scale; **FTG**: 1.0 mm Wire-bond fine-pitch; **SBG / SBV**: 0.8 mm Lidless flip-chip; **FGG**: 1.0 mm Wire-bond fine-pitch; **FBG / FBV** 1.0 mm Lidless flip-chip; **FFG / FFV**: 1.0 mm Flip-chip fine-pitch

Notes: 1. Supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates.
2. Represents the maximum number of transceivers available. Note that the majority of devices are available without transceivers. See the Package section of this table for details.
3. Leaded package option available for all packages. See DS180, *7 Series FPGAs Overview* for details.
4. Device migration is available within the Artix-7 family for like packages but is not supported between other 7 series families.

Zynq-7000 AP SoCs

		Low-End Portfolio			Mid-Range Devices			
	Device Name	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
	Part Number	XC7Z010	XC7Z015	XC7Z020	XC7Z030	XC7Z035	XC7Z045	XC7Z100
Processing System	Processor Core	Dual ARM® Cortex™-A9 MPCore™ with CoreSight™						
	Processor Extensions	NEON™ & Single / Double Precision Floating Point for each processor						
	Maximum Frequency	866MHz			Up to 1GHz(1)			
	L1 Cache	32KB Instruction, 32KB Data per processor						
	L2 Cache	512KB						
	On-Chip Memory	256KB						
	External Memory Support(2)	DDR3, DDR3L, DDR2, LPDDR2						
	External Static Memory Support(2)	2x Quad-SPI, NAND, NOR						
	DMA Channels	8 (4 dedicated to Programmable Logic)						
	Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO						
	Peripherals w/ built-in DMA(2)	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO						
	Security(3)	RSA Authentication of First Stage Boot Loader, AES and SHA 256b Decryption and Authentication for Secure Boot						
	Processing System to Programmable Logic Interface Ports (Primary Interfaces & Interrupts Only)	2x AXI 32b Master, 2x AXI 32b Slave 4x AXI 64b/32b Memory AXI 64b ACP 16 Interrupts						
Programmable Logic	7 Series Programmable Logic Equivalent	Artix®-7 FPGA	Artix-7 FPGA	Artix-7 FPGA	Kintex®-7 FPGA	Kintex-7 FPGA	Kintex-7 FPGA	Kintex-7 FPGA
	Logic Cells (Approximate ASIC Gates(4))	28K (~430K)	74K (~1.1M)	85K (~1.3M)	125K (~1.9M)	275K (~4.1M)	350K (~5.2M)	444K (~6.6M)
	Look-Up Tables (LUTs)	17,600	46,200	53,200	78,600	171,900	218,600	277,400
	Flip-Flops	35,200	92,400	106,400	157,200	343,800	437,200	554,800
	Total Block RAM (# 36Kb Blocks)	2.1Mb (60)	3.3Mb (95)	4.9Mb (140)	9.3Mb (265)	17.6Mb (500)	19.1Mb (545)	26.5Mb (755)
	Programmable DSP Slices (18x25 MACCs)	80	160	220	400	900	900	2,020
	Peak DSP Performance (Symmetric FIR)	100 GMACs	200 GMACS	276 GMACs	593 GMACs	1,334 GMACs	1,334 GMACs	2,622 GMACs
	PCI Express® (Root Complex or Endpoint)	—	Gen2 x4	—	Gen2 x4	Gen2 x8	Gen2 x8	Gen2 x8
	Analog Mixed Signal (AMS) / XADC(2)	2x 12 bit, MSPS ADCs with up to 17 Differential Inputs						
	Security(3)	AES and SHA 256b Decryption and Authentication for Secure Programmable Logic Configuration						

1. 1 GHz processor frequency is available only for -3 speed grades for devices in flip-chip packages. Please see the data sheet for more details.
2. Z-7010 in CLG225 has restrictions on PS peripherals, memory interfaces, and I/Os. Please refer to the Technical Reference Manual for more details.
3. Security block is shared by the Processing System and the Programmable Logic.
4. Equivalent ASIC gate count is dependent of the function implemented. The assumption is 1 Logic Cell = ~15 ASIC Gates.

Zynq-7000 AP SoCs
HR I/O, PS I/O, and Transceivers (GTP or GTX)

		Low-End Portfolio			Mid-Range Devices			
	Device Name	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
	Part Number	XC7Z010	XC7Z015	XC7Z020	XC7Z030	XC7Z035	XC7Z045	XC7Z100
Unique Footprint	PCB Footprint Dimensions (mm) [1]	GTP Transceivers			GTX Transceivers			
CLG225	13x13	54[2], 86, 0						
CLG400	17x17	100, 128, 0		128, 128, 0				
CLG484	19x19							
CLG485[3]	19x19		150, 128, 4					
SBG485 / SBV485[3]	19x19				50[2], 128, 4			
FBG484 / FBV484	23x23				100, 128, 4			
FBG676 / FBV676[1]	27x27				100, 128, 4	100, 128, 8	100, 128, 8	
FFG676 / FFV676[1]	27x27				100, 128, 4	100, 128, 8	100, 128, 8	
FFG900 / FFV900	31x31					212, 128, 16	212, 128, 16	212, 128, 16
FFG1156 / FFV1156	35x35							250, 128, 16

1. Devices in the same package are footprint compatible. FBG676 / FBV676 and FFG676 / FFV676 are also footprint compatible.
2. Static memory interface combined with the usage of many peripherals could require more than 50 I/Os. In that case, the designer can use the Programmable Logic SelectIO interface.
3. CLG485 and SBG485 / SBV485 are pin-to-pin compatible. See product data sheets and user guides for more details.
   See DS190, *Zynq-7000 All Programmable SoC Overview* for package details.

Device Ordering Information

SPARTAN-6

XC	6	S	LX / LXT	###	-1	FB	900	C
Xilinx Commercial	Generation	Family	Sub-families	Logic Cells In 1K units	Speed Grade -L1 = Low Power -2 = Mid -3 = Highest	Footprint Package Type CP: Wire-bond (.5mm) TQ: Quad Flat Pack (.5mm) CS: Wire-bond (.8mm) FT: Wire-bond (1mm) FG: Wire-bond (1mm)	Footprint Package Pin Count	Temperature Grade (C, E, I)

ARTIX-7

XC	7	A	###	-1	FF	V	900	C
Xilinx Commercial	Generation	Family	Logic Cells In 1K units	Speed Grade -1 = Slowest -L1 = Low Power -L2 = Low Power -2 = Mid -3 = Highest	Package Type FB: Lidless Flip Chip (1mm) FF: Flip-chip (1mm)	Footprint V: RoHS 6/6 G: RoHS 6/6 w/exemption 15	Nominal Package Pin Count	Temperature Grade (C, E, I)

ZYNQ-7000

XC	7	Z	###	-1	FF	V	###	C
Xilinx Commercial	Generation	Zynq	Value Index	Speed Grade -1: Slowest -L1: Low Power -2: Mid -L2: Low Power -3: Fastest	CL: Wire-bond Lidded w/1.0mm Ball Pitch SB: Flip-chip Lidless w/ 0.8mm Ball Pitch FF: Flip-chip Lidded w/ 1.0mm Ball Pitch FB: Flip-chip Lidless w/ 1.0mm Ball Pitch	V: RoHS 6/6 G (CLG) = RoHS 6/6 G (SBG, FBG, FFG) = RoHS 6/6 with exemption 15	Footprint Package Pin Count	Temperature Grade (C, E, I)

Notes:
-L1 is the ordering code for the lower power, -1L speed grade.
-L2 is the ordering code for the lower power, -2L speed grade.
C = Commercial (Tj = 0°C to +85°C) E = Extended (Tj = 0°C to +100°C) I = Industrial (Tj = –40°C to +100°C)

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

Spartan®-6 Device Footprint Compatibility

8mm–31mm

I/O, GTP Transceivers

Dimensions (mm)	8x8	13x13	15x15	17x17	19x19	20x20	23x23	27x27	31x31
Unique Footprint	CPG196	CSG225	CSG324	FTG256	CSG484	TQG144	FGG484	FGG676	FGG900
6SLX4	106, 0	132, 0				102, 0			
6SLX9	106, 0	160, 0	200, 0	186, 0		102, 0			
6SLX16	106, 0	160, 0	232, 0	186, 0					
6SLX25			226, 0	186, 0			266, 0		
6SLX45			218, 0		320, 0		316, 0	358, 0	
6SLX75					328, 0		280, 0	408, 0	
6SLX100					338, 0		326, 0	480, 0	
6SLX150					338, 0		338, 0	498, 0	576, 0

Dimensions (mm)			15x15		19x19		23x23	27x27	31x31
Unique Footprint			CSG324		CSG484		FGG484	FGG676	FGG900
6SLX25T			190, 2				250, 2		
6SLX45T			190, 4		296, 4		295, 4		
6SLX75T					292, 4		268, 4	348, 8	
6SLX100T					296, 4		296, 4	376, 8	498, 8
6SLX150T					296, 4		296, 4	396, 8	540, 8

The footprint compatibility range is indicated by shading per column.

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

Artix®-7 Device Footprint Compatibility

10mm–35mm

HR I/O, GTP Transceivers

PCB Footprint Dimensions (mm)	10x10	15x15	15x15	17x17	19x19	23x23	23x23	27x27	27x27	35x35
Unique Footprint	CPG236	CSG324	CSG325	FTG256	SBG484 SBV484	FBG484 FBV484	FGG484	FBG676 FBV676	FGG676	FFG1156 FFV1156
7A15T	106, 2	210, 0	150, 4	170, 0			250, 4			
7A35T	106, 2	210, 0	150, 4	170, 0			250, 4			
7A50T	106, 2	210, 0	150, 4	170, 0			250, 4			
7A75T		210, 0		170, 0			285, 4		300, 8	
7A100T		210, 0		170, 0			285, 4		300, 8	
7A200T					285, 4	285, 4		400, 8		500, 16

The footprint compatibility range is indicated by shading per column.

Zynq®-7000 Device Footprint Compatibility

13mm–35mm

HR I/O, PS I/O, and GTP Transceivers

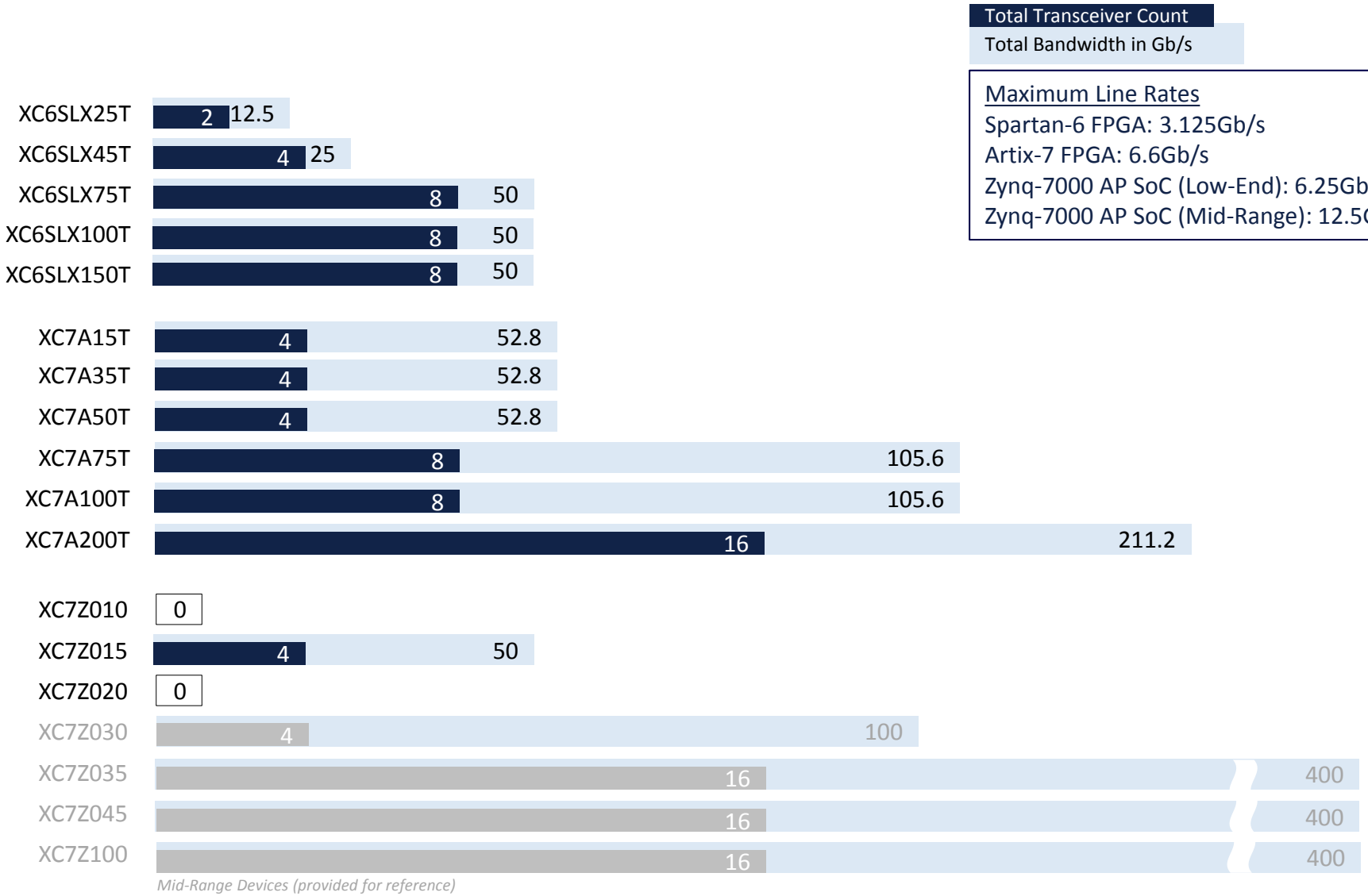
PCB Footprint Dimensions (mm)	13x13	17x17	19x19	19x19	23x23	27x27	27x27	31x31	35x35
Unique Footprint	CLG225	CLG400	CLG484	CLG485	FBG484	FBG676	FFG676	FFG900	FFG1156
7Z010	54, 86, 0	100, 130, 0							
7Z015				150, 130, 4					
7Z020		125, 130, 0	200, 130, 0						
Mid-Range Devices (provided for reference) *HR I/O, HP I/O, PS I/O, GTX Transceivers*									
7Z030				*50, 100, 130, 4*	*100, 63, 130, 4*	*100, 150, 130, 4*	*100, 150, 130, 4*		
7Z035						*100, 150, 130, 8*	*100, 150, 130, 8*	*212, 150, 130, 16*	
7Z045						*100, 150, 130, 8*	*100, 150, 130, 8*	*212, 150, 130, 16*	
7Z100								*212, 150, 130, 16*	*250, 150, 130, 16*

The footprint compatibility range is indicated by shading per column.

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

Transceiver Count and Bandwidth

SPARTAN 6 ARTIX 7 ZYNQ



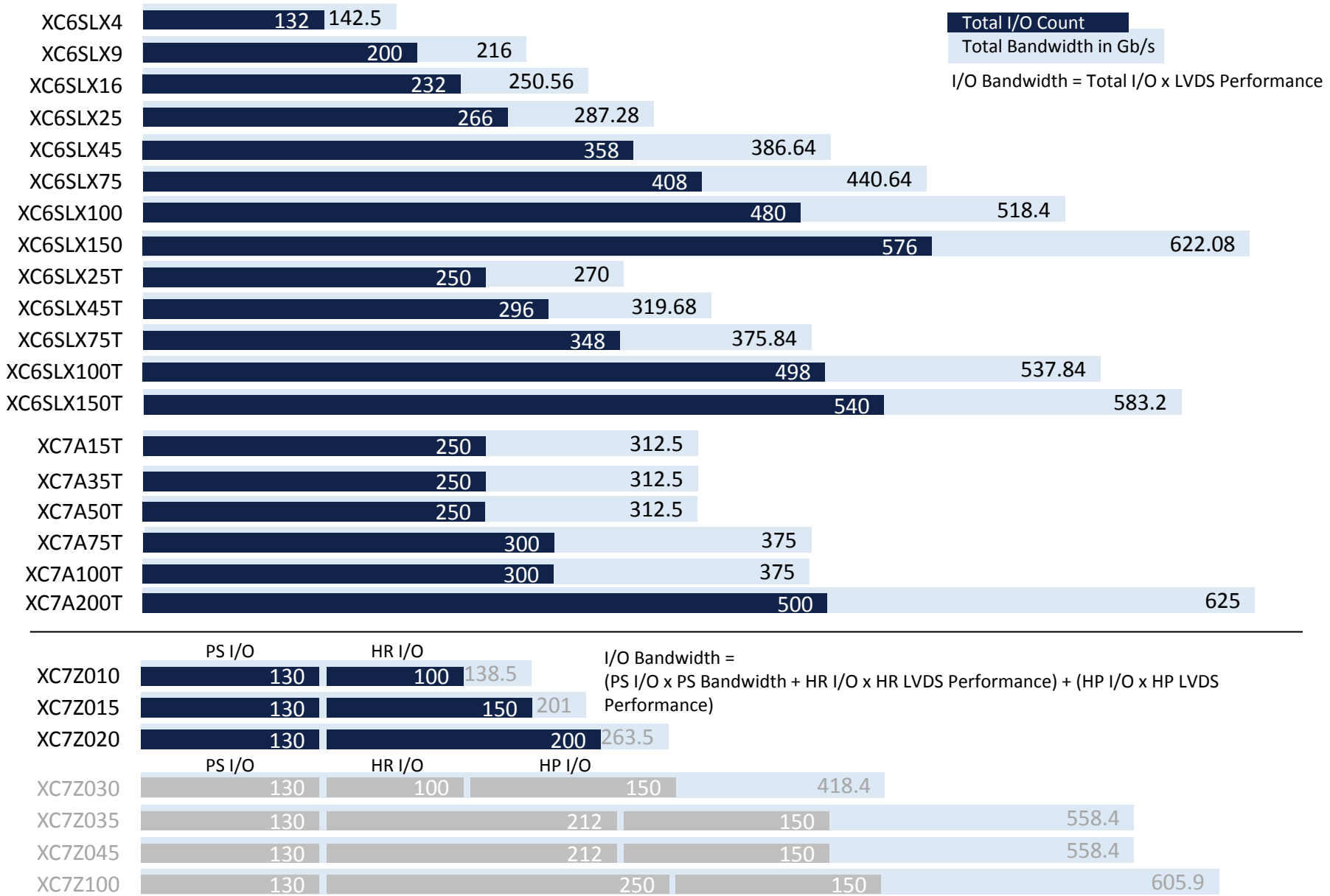
Maximum Line Rates
Spartan-6 FPGA: 3.125Gb/s
Artix-7 FPGA: 6.6Gb/s
Zynq-7000 AP SoC (Low-End): 6.25Gb/s
Zynq-7000 AP SoC (Mid-Range): 12.5Gb/s

Transceiver Bandwidth = (Total Transceiver Count x Maximum Line Rate) x 2

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

I/O Count and Bandwidth

SPARTAN 6 ARTIX 7 ZYNQ



Zynq®-7000 AP SoCs: Dedicated DDR I/O bandwidth not included.

Important: Verify all data in this document with the device data sheets found at www.xilinx.com.

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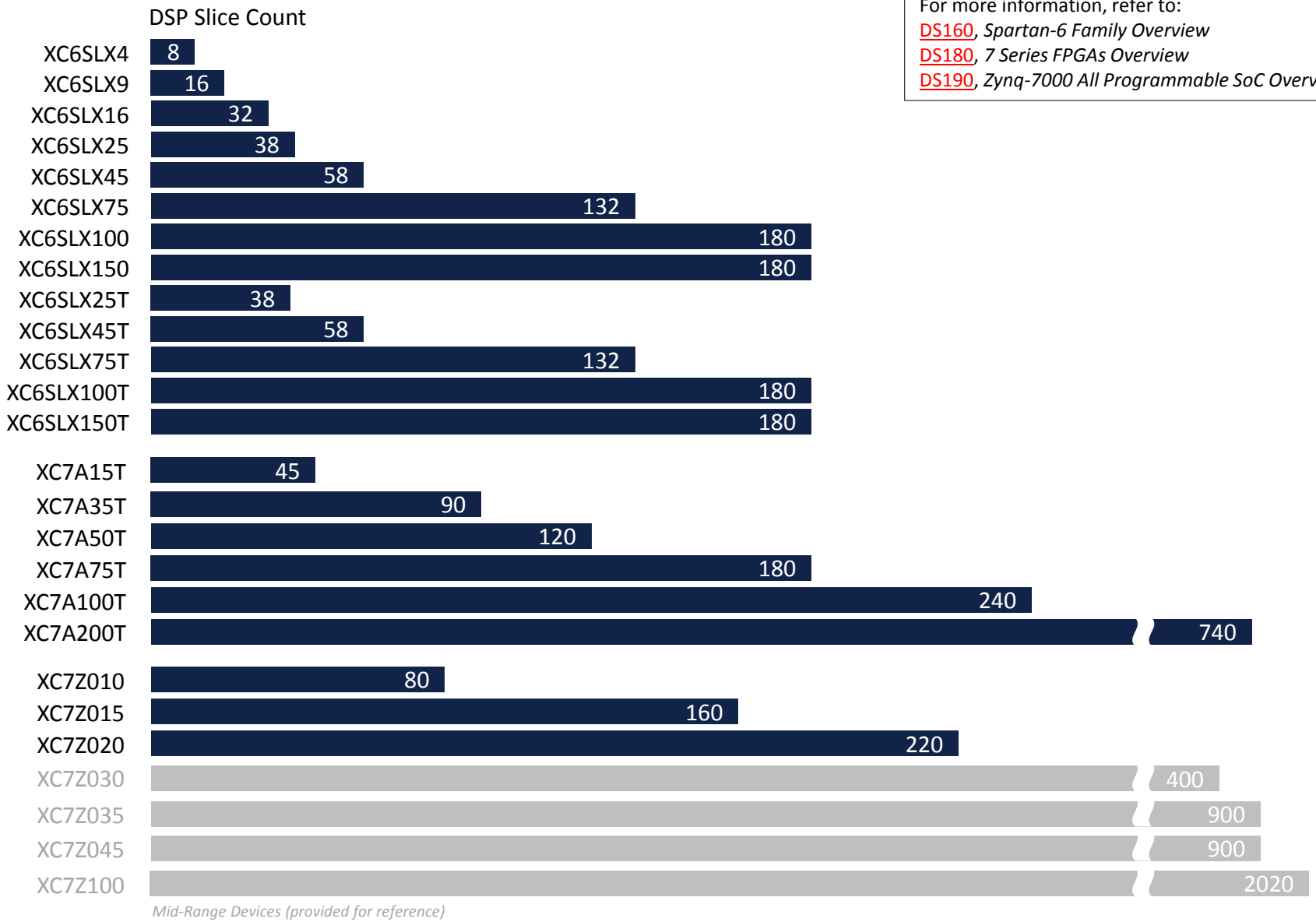
Digital Signal Processing Metrics

SPARTAN 6 ARTIX 7 ZYNQ

For more information, refer to:
DS160, *Spartan-6 Family Overview*
DS180, *7 Series FPGAs Overview*
DS190, *Zynq-7000 All Programmable SoC Overview*

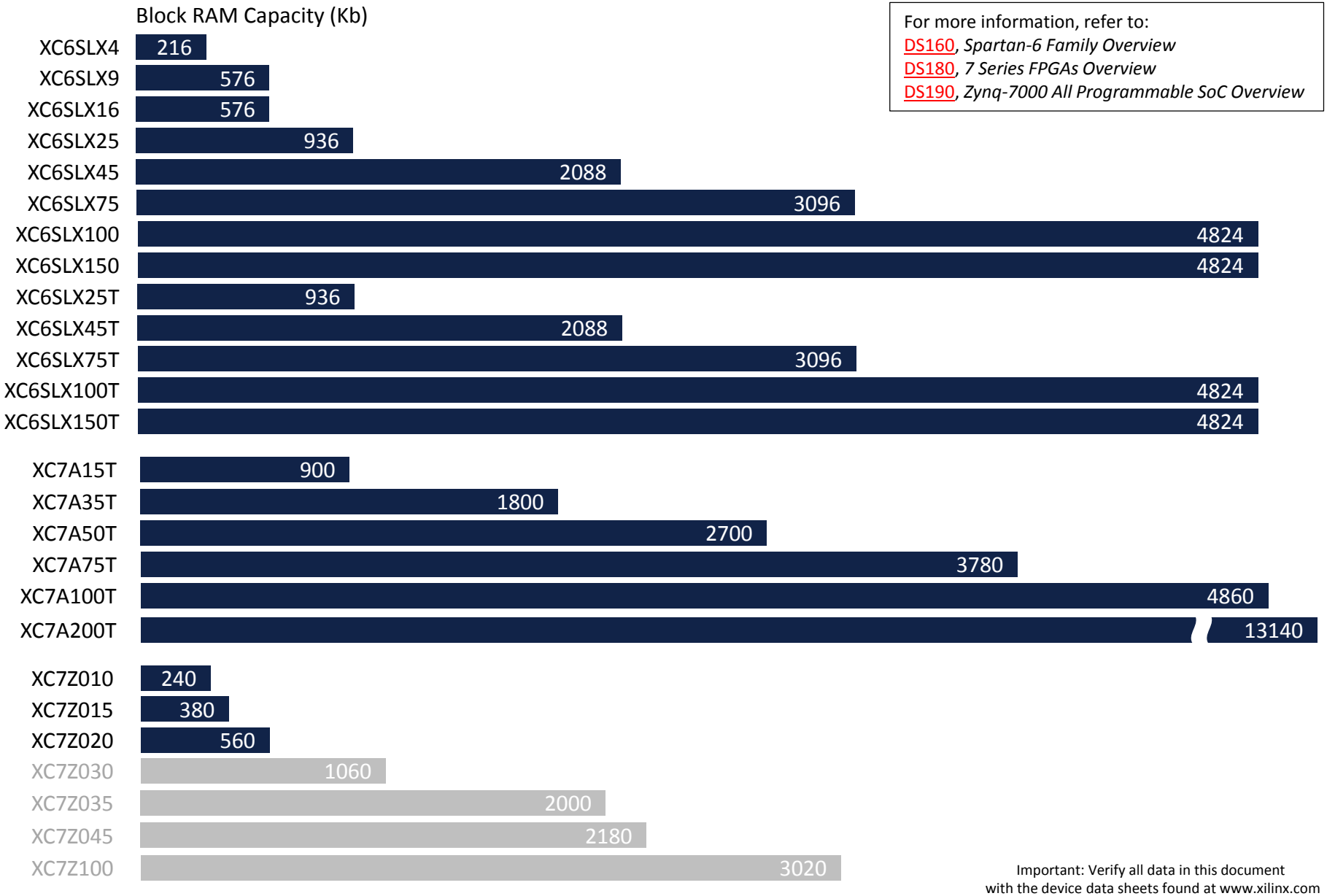


Mid-Range Devices (provided for reference)

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

Block RAM Metrics

SPARTAN 6 ARTIX 7 ZYNQ



For more information, refer to:
DS160, *Spartan-6 Family Overview*
DS180, *7 Series FPGAs Overview*
DS190, *Zynq-7000 All Programmable SoC Overview*

Mid-Range Devices (provided for reference)

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

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References

Spartan®-6 Product Page

DS160, *Spartan-6 Family Overview*

DS162, *Spartan-6 FPGA Data Sheet: DC and Switching Characteristics*

Artix®-7 FPGA Product Page

DS180, *7 Series FPGAs Overview*

DS181, *Artix®-7 FPGAs Data Sheet: DC and Switching Characteristics*

Zynq®-7000 Product Page

DS190, *Zynq-7000 All Programmable SoC Overview*

DS187, *Zynq-7000 All Programmable SoC (Z-7010, Z-7015, and Z-7020): DC and AC Switching Characteristics*